

SL3S1205_15

UCODE 8/8m

Rev. 3.5 — 1 April 2021

398435

Product data sheet
COMPANY PUBLIC

1 General description

The UCODE 8 and UCODE 8m ICs are the latest NXP products of the UCODE family. UCODE 8/8m offers high performance and features for use in the most demanding RFID tagging applications.

Particularly well suited for inventory management applications, like e.g Retail and Fashion, with its great RF performance for any given form factor, UCODE 8/8m enables long read distance and fast inventory of dense RFID tag population. With its broadband design, it offers the possibility to manufacture true global RFID label with great performance over worldwide regulations.

The device also provides a Self Adjust Feature, a Product Status Flag for Electronic Article Surveillance (EAS) application, pre-serialized 96-bit EPC, Brand Identifier and the EPC Gen2v2 compliant Untraceable command.



2 Features and benefits

2.1 Key features

- Read sensitivity -23 dBm
- Write sensitivity -18 dBm
- Innovative functionality
 - Self Adjust
 - Memory Safeguard
 - Brand Identifier
 - Untraceable
 - Pre-serialization for 96-bit EPC
 - Integrated Product Status Flag (PSF)
- Compatible with single-slit antenna
- Up to 128-bit EPC
- 96-bit Unique Tag Identifier (TID) factory locked, including 48-bit unique serial number
- EPC Gen2v2

2.1.1 Memory

- 128-bit/96-bit (UCODE 8/UCODE 8m) of EPC memory
- Supports pre-serialization for 96-bit EPC
- 96-bit Tag Identifier (TID) factory locked
- 48-bit unique serial number factory-encoded into TID
- 0-bit/32-bit (UCODE 8/UCODE 8m) User Memory
- 32-bit kill password to permanently disable the tag
- 32-bit access password
- Wide operating temperature range: -40 °C up to +85 °C
- Minimum 100k write cycle endurance

2.2 Supported features

- All mandatory commands of EPC global specification V.2.0.1 are implemented including:
 - Lock or permalock
 - Kill Command
- The following optional commands are implemented in conformance with the EPC specification:
 - Access
 - BlockWrite (2 words, 32-bit)
 - Untraceable
- Product Status Flag bit: enables the UHF RFID tag to be used as EAS (Electronic Article Surveillance) tag without the need for a back-end database.
- Self Adjust for automated tag performance optimization
- Memory Safeguard: enables countermeasures, like parity and margin checks as well as automated error correction, to ensure integrity of customer data.
- Brand Identifier: enables product authentication verification

All supported features of UCODE 8/8m can be activated using standard EPCglobal READ / WRITE / ACCESS / SELECT commands. No custom commands are needed to take advantage of all the features.

3 Applications

3.1 Target market

- Retail
 - Brick and mortar
 - e-commerce
 - omnichannel
- Supply chain management
- Shipping services
- Airline luggage tracking
- Laundry services

3.2 Applications

- High accurate and fast inventory management, enabling omnichannel retail processes
- Tracking along the supply chain from source to store
- High-speed store checkout process, bringing convenience to the customer
- Loss prevention
- Brand Protection
- After sales operations: Return and Warranty management

Outside the applications mentioned above, please contact NXP Semiconductors for support.

4 Ordering information

Table 1. Ordering information

Type number	Package			
	Name	IC type	Description	Version
SL3S1205FUD/HA	Wafer	UCODE 8	Die on sawn 8" 120 μm wafer 10 μm Polyimide spacer with Large Pads, Stealth Dicing	not applicable
SL3S1215FUD/HA	Wafer	UCODE 8m	Die on sawn 8" 120 μm wafer 10 μm Polyimide spacer with Large Pads, Stealth Dicing	not applicable
SL3S1205FUD2/HA	Wafer	UCODE 8	Die on sawn 12" 120 μm wafer 10 μm Polyimide spacer with Large Pads, Conventional Dicing	not applicable
SL3S1215FUD2/HA	Wafer	UCODE 8m	Die on sawn 12" 120 μm wafer 10 μm Polyimide spacer with Large Pads, Conventional Dicing	not applicable
SL3S1205FUD2/HAP	Wafer	UCODE 8	Die on sawn 12" 120 μm wafer 10 μm Polyimide spacer with Large Pads, Plasma Dicing	not applicable
SL3S1215FUD2/HAP	Wafer	UCODE 8m	Die on sawn 12" 120 μm wafer 10 μm Polyimide spacer with Large Pads, Plasma Dicing	not applicable

5 Block diagram

The UCODE 8/8m IC consists of three major blocks:

- Analog Interface
- Digital Control
- EEPROM

The analog part provides stable supply voltage and demodulates data received from the reader which is then processed by the digital part. Further, the modulation transistor of the analog part transmits data back to the reader.

The digital section includes the state machines, processes the protocol and handles communication with the EEPROM, which contains the EPC and the user data.

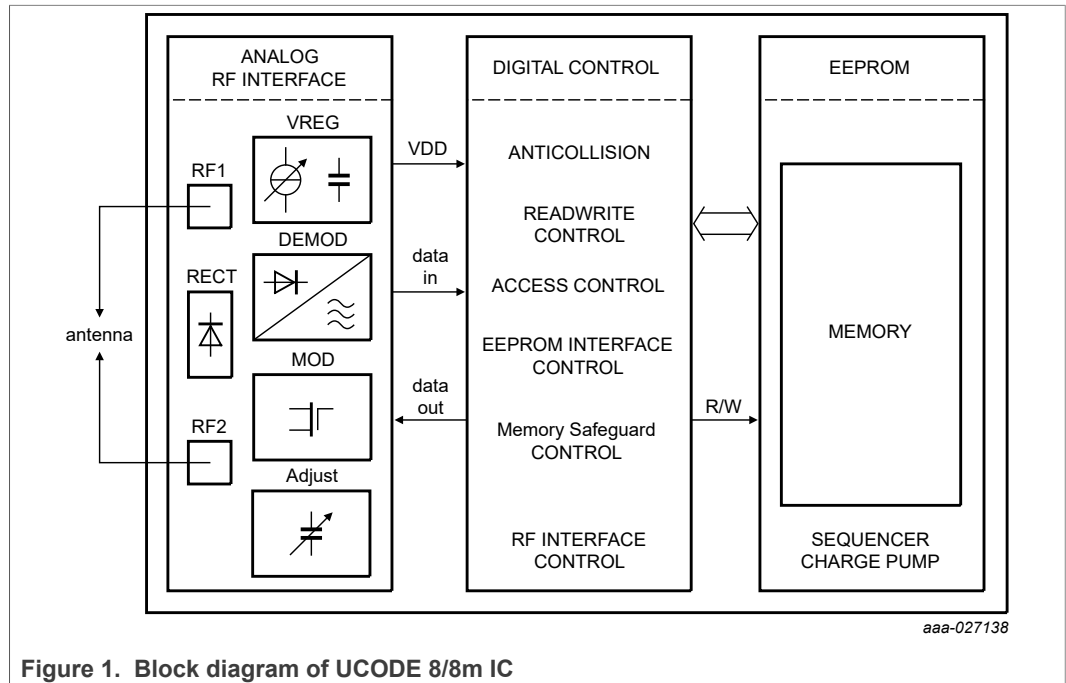
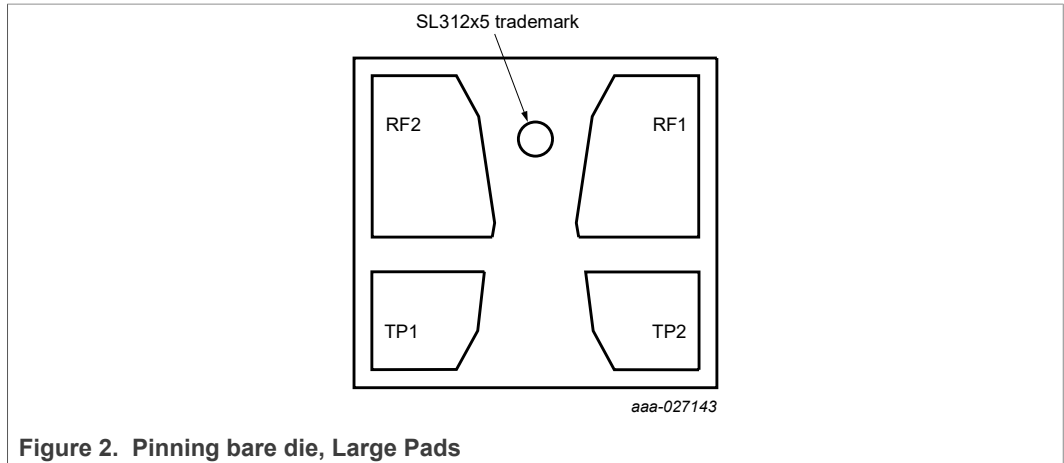


Figure 1. Block diagram of UCODE 8/8m IC

6 Pinning information

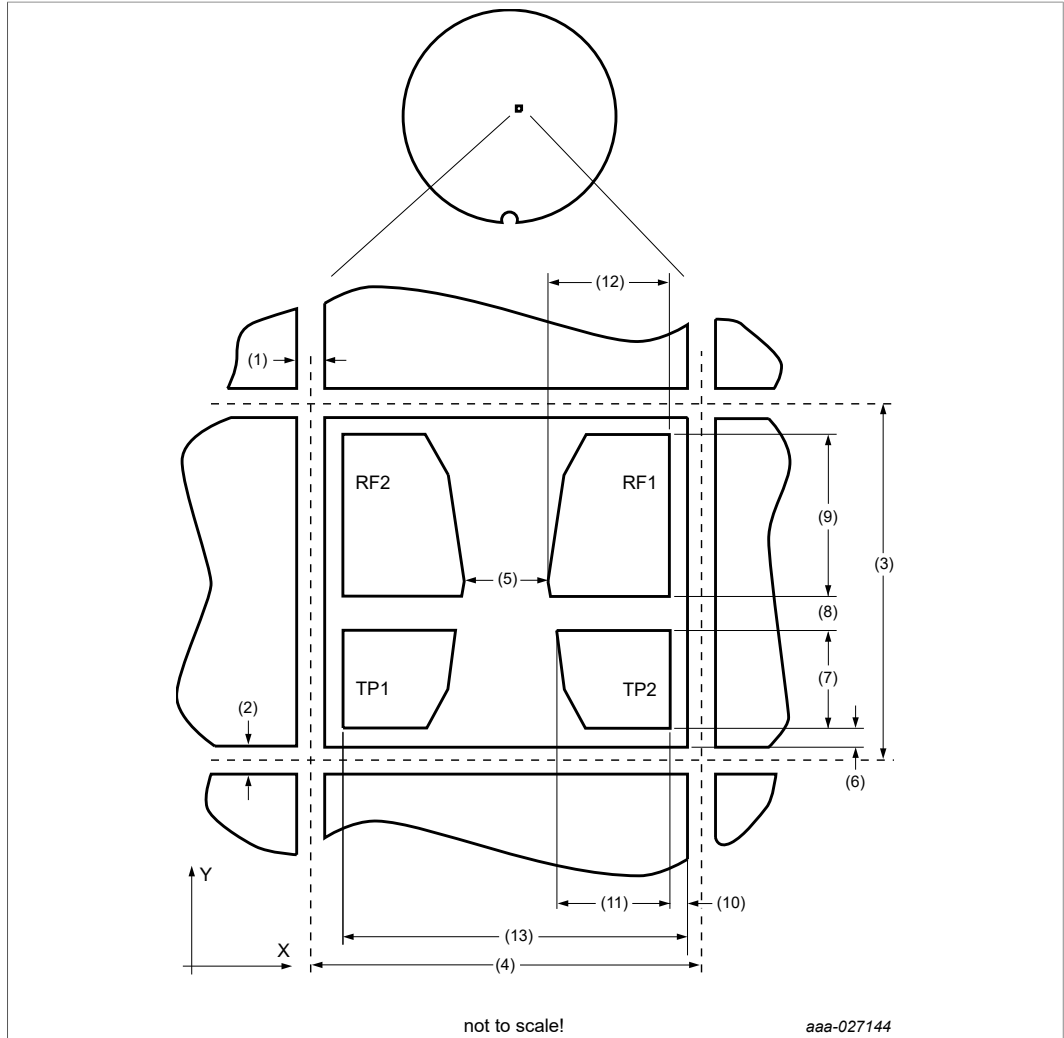


6.1 Pin description

Table 2. Pin description bare die

Symbol	Description
TP1	test pad 1
RF1	antenna connector 1
TP2	test pad 2
RF2	antenna connector 2

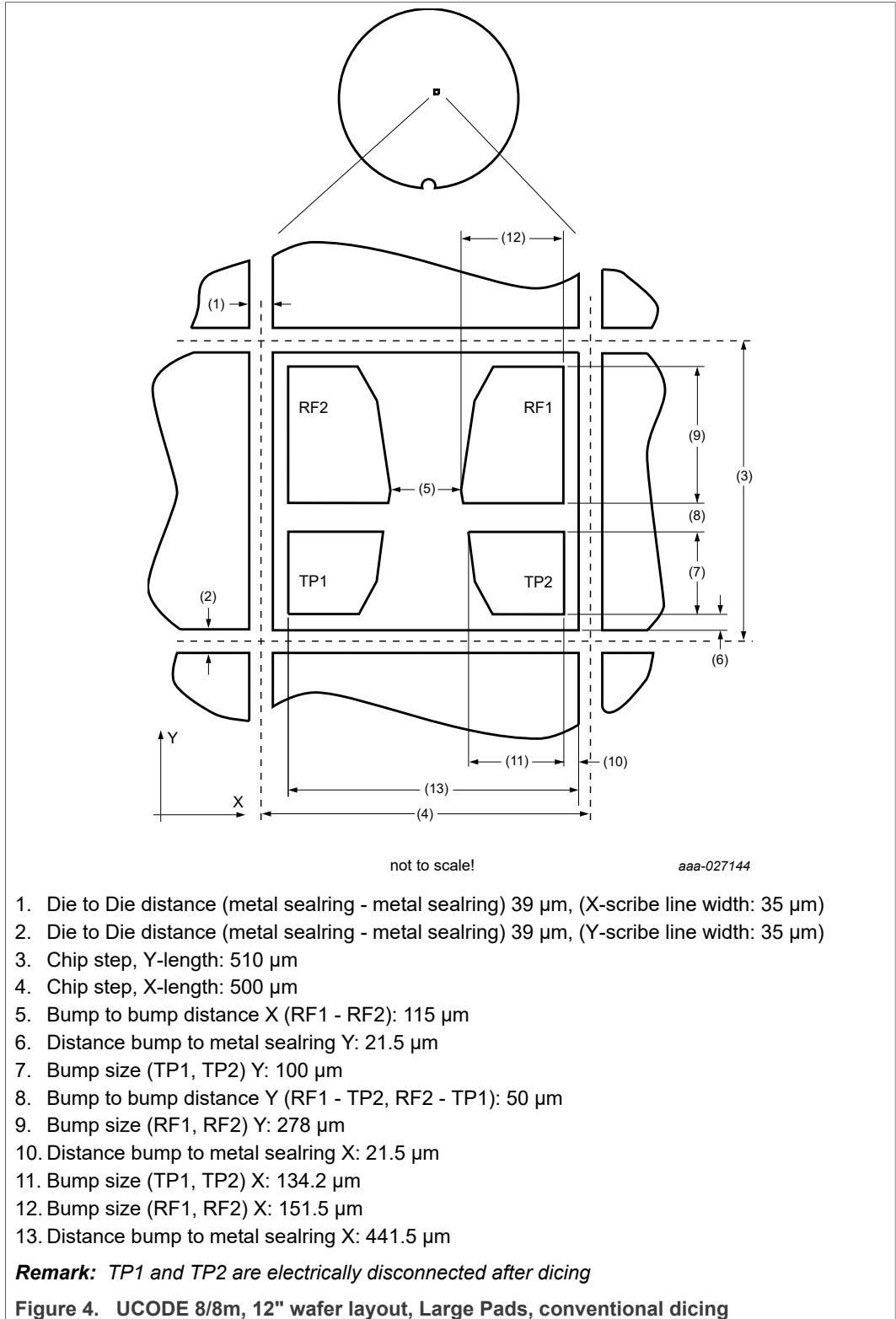
7 Wafer layout

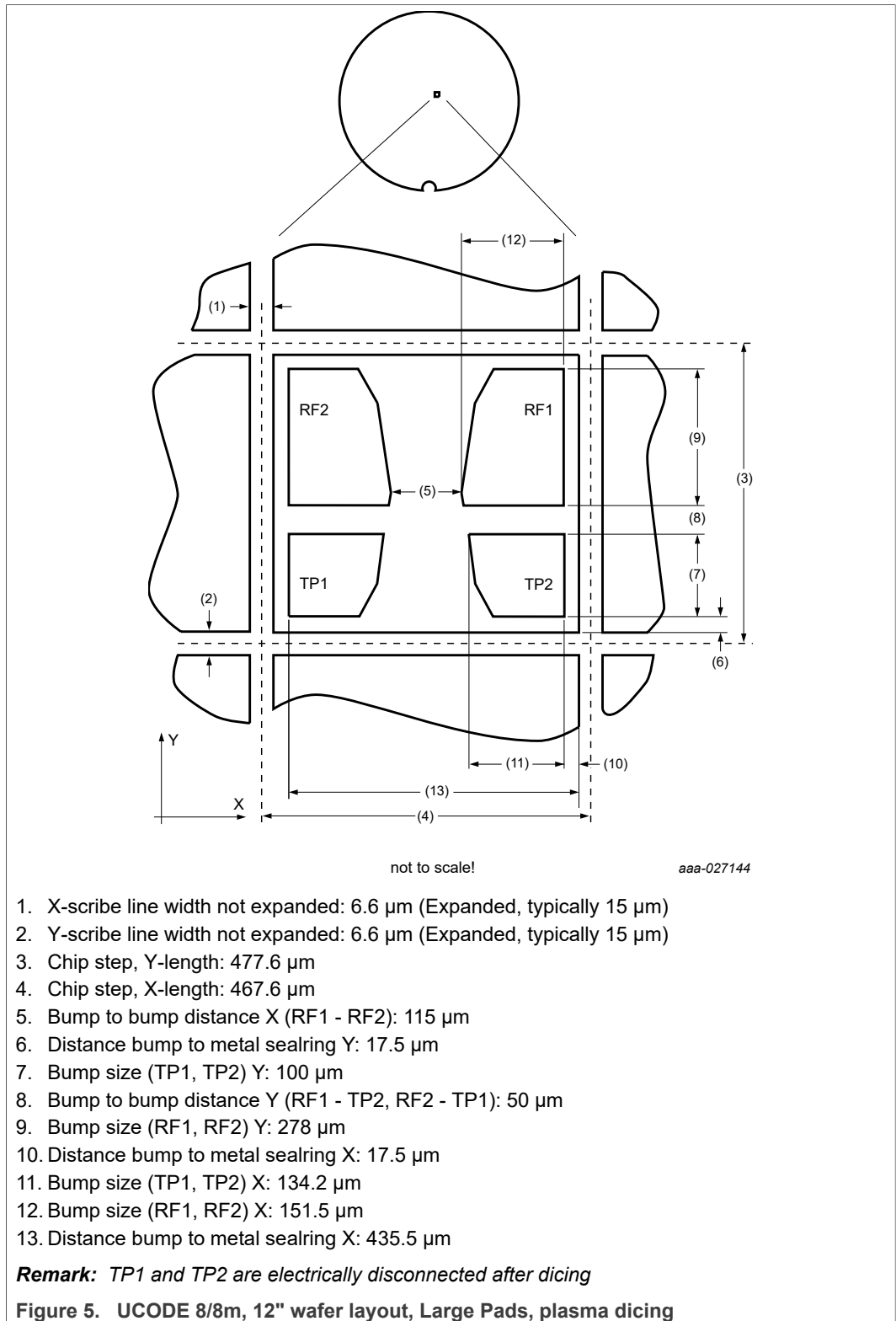


- 1. Die to Die distance (metal searing - metal searing) 19 μm , (X-scribe line width: 15 μm)
- 2. Die to Die distance (metal searing - metal searing) 19 μm , (Y-scribe line width: 15 μm)
- 3. Chip step, Y-length: 490 μm
- 4. Chip step, X-length: 480 μm
- 5. Bump to bump distance X (RF1 - RF2): 115 μm
- 6. Distance bump to metal searing Y: 21.5 μm
- 7. Bump size (TP1, TP2) Y: 100 μm
- 8. Bump to bump distance Y (RF1 - TP2, RF2 - TP1): 50 μm
- 9. Bump size (RF1, RF2) Y: 278 μm
- 10. Distance bump to metal searing X: 21.5 μm
- 11. Bump size (TP1, TP2) X: 134.2 μm
- 12. Bump size (RF1, RF2) X: 151.5 μm
- 13. Distance bump to metal searing X: 441.5 μm

Remark: TP1 and TP2 are electrically disconnected after dicing

Figure 3. UCODE 8/8m, 8" wafer layout, Large Pads, stealth dicing





8 Mechanical specification

The UCODE 8 wafers are available in 120 μm thickness. For Large Gold Pads the 120 μm thick wafer is enhanced with 10 μm Polyimide spacer resulting in less coupling between the antenna and the active circuit, leaving a larger process window for assembly.

8.1 Wafer specification

8.1.1 8 inch Wafer with Large Pads, stealth dicing

See ["Data sheet - Delivery type description – General specification for 8" wafer on UV-tape with electronic fail die marking, BU-S&C document number: 1093**"](#)

Table 3. 8 inch specification with Large Pads, stealth dicing

Wafer	
Designation	each wafer is scribed with batch number and wafer number
Diameter	200 mm (8") unsawn- 205 mm typical sawn on foil
Thickness	120 $\mu\text{m} \pm 15 \mu\text{m}$
Number of pads	4
Pad location	non-diagonal / placed in chip corners
Process	CMOS 0.14 μm
Batch size	25 wafers
Net printed dies per wafer	120794
Wafer backside	
Material	Si
Treatment	ground and stress release
Roughness	R_a max. 0.5 μm , R_t max. 5 μm
Chip dimensions	
Die size excluding scribe	0.465 mm \times 0.475 mm = 0.22 mm ²
Scribe line width:	x-dimension = 15 μm y-dimension = 15 μm
Passivation on front	
Type	Sandwich structure
Material	PE-Nitride (on top)
Thickness	1.75 μm total thickness of passivation
Polyimide spacer	10 $\mu\text{m} \pm 2 \mu\text{m}$
Au pads	
Pad material	> 99.9 % pure Au
Pad hardness	35 – 80 HV 0.005

Table 3. 8 inch specification with Large Pads, stealth dicing...continued

Pad shear strength	> 70 MPa
Pad height	3 μm
Pad height uniformity	
– within a die	max. 2 μm
– within a wafer	max. 4 μm
Pad flatness	max. 3 μm
Pad size	
– RF1, RF2 (max. details see wafer layout)	151.5 μm \times 278 μm
– TP1, TP2 (max. details see wafer layout)	134.2 μm \times 100 μm
Pad size variation	\pm 5 μm

8.1.2 12 inch Wafer with Large Pads

See ["Data sheet - Delivery type description – General specification for 12" wafer on UV-tape with electronic fail die marking, BU-S&C document number: 1862***"](#)

Table 4. 12 inch specification with Large Pads, conventional dicing

Wafer	
Designation	each wafer is scribed with batch number and wafer number
Diameter	300 mm (12") unsawn
Thickness	120 μm \pm 15 μm
Number of pads	4
Pad location	non-diagonal / placed in chip corners
Process	CMOS 0.14 μm
Batch size	25 wafers
Net printed dies per wafer	258934
Wafer backside	
Material	Si
Treatment	ground and stress release
Roughness	R_a max. 0.5 μm , R_t max. 5 μm
Chip dimensions	
Die size excluding scribe	0.465 mm \times 0.475 mm = 0.22 mm ²
Scribe line width:	x-dimension = 35 μm
	y-dimension = 35 μm
Passivation on front	
Type	Sandwich structure
Material	PE-Nitride (on top)
Thickness	1.75 μm total thickness of passivation
Polyimide spacer	10 μm \pm 2 μm

Table 4. 12 inch specification with Large Pads, conventional dicing ...continued

Au pads	
Pad material	> 99.9 % pure Au
Pad hardness	35 – 80 HV 0.005
Pad shear strength	> 70 MPa
Pad height	3 μ m
Pad height uniformity	
– within a die	max. 2 μ m
– within a wafer	max. 4 μ m
Pad flatness	max. 3 μ m
Pad size	
– RF1, RF2 (max. details see wafer layout)	151.5 μ m \times 278 μ m
– TP1, TP2 (max. details see wafer layout)	134.2 μ m \times 100 μ m
Pad size variation	\pm 5 μ m

Table 5. 12 inch specification with Large Pads, plasma dicing

Wafer	
Designation	each wafer is scribed with batch number and wafer number
Diameter	300 mm (12") unsawn
Thickness	120 μ m \pm 15 μ m
Number of pads	4
Pad location	non-diagonal / placed in chip corners
Process	CMOS 0.14 μ m
Batch size	25 wafers
Net printed dies per wafer	296307
Wafer backside	
Material	Si
Treatment	ground and stress release
Roughness	R _a max. 0.5 μ m, R _t max. 5 μ m
Chip dimensions	
Die size excluding scribe	0.461 mm \times 0.471 mm = 0.22 mm ²
Scribe line width:	x-dimension = 6.6 μ m
	y-dimension = 6.6 μ m
Passivation on front	
Type	Sandwich structure
Material	PE-Oxide (on top)
Thickness	2.25 μ m total thickness of passivation

Table 5. 12 inch specification with Large Pads, plasma dicing ...continued

Polyimide spacer	10 $\mu\text{m} \pm 2 \mu\text{m}$
Au pads	
Pad material	> 99.9 % pure Au
Pad hardness	35 – 80 HV 0.005
Pad shear strength	> 70 MPa
Pad height	3 μm
Pad height uniformity	
– within a die	max. 2 μm
– within a wafer	max. 4 μm
Pad flatness	max. 3 μm
Pad size	
– RF1, RF2 (max. details see wafer layout)	151.5 $\mu\text{m} \times 278 \mu\text{m}$
– TP1, TP2 (max. details see wafer layout)	134.2 $\mu\text{m} \times 100 \mu\text{m}$
Pad size variation	$\pm 5 \mu\text{m}$

8.1.3 Fail die identification

No ink dots are applied to the wafer.

Electronic wafer mapping (SECS II format) covers the electrical test results and additionally the results of mechanical/visual inspection.

See ["Data sheet - Delivery type description – General specification for 8" wafer on UV-tape with electronic fail die marking, BU-S&C document number: 1093**"](#)

See ["Data sheet - Delivery type description – General specification for 12" wafer on UV-tape with electronic fail die marking, BU-S&C document number: 1862**"](#)

8.1.4 Map file distribution

See ["Data sheet - Delivery type description – General specification for 8" wafer on UV-tape with electronic fail die marking, BU-S&C document number: 1093**"](#)

See ["Data sheet - Delivery type description – General specification for 12" wafer on UV-tape with electronic fail die marking, BU-S&C document number: 1862**"](#)

9 Functional description

9.1 Air interface standards

The UCODE 8/8m fully supports all parts of the "EPCTM Radio-Frequency Identity Protocols Generation-2 UHF RFID, Specification for RFID Air Interface, Protocol for Communications at 860 MHz to 960 MHz, Version 2.0.1".

9.2 Power transfer

The interrogator provides an RF field that powers the tag, equipped with a UCODE 8/8m. The antenna transforms the impedance of free space to the chip input impedance in order to get the maximum power for the UCODE 8/8m on the tag.

The RF field, which is oscillating on the operating frequency provided by the interrogator, is rectified to provide a smoothed DC voltage to the analog and digital modules of the IC.

The antenna that is attached to the chip may use a DC connection between the two antenna pads. Therefore the UCODE 8/8m also enables loop antenna design.

9.3 Data transfer

9.3.1 Interrogator to tag Link

An interrogator transmits information to the UCODE 8/8m by modulating an UHF RF signal. The UCODE 8/8m receives both information and operating energy from this RF signal. Tags are passive, meaning that they receive all of their operating energy from the interrogator's RF waveform.

An interrogator is using a fixed modulation and data rate for the duration of at least one inventory round. It communicates to the UCODE 8/8m by modulating an RF carrier.

For further details, refer to ["Interrogator-to-tag \(R=>T\) communications"](#)

9.3.2 Tag to interrogator Link

Upon transmitting a valid command, an interrogator receives information from a UCODE 8/8m tag by transmitting an unmodulated RF carrier and listening for a backscattered reply. The UCODE 8/8m backscatters by switching the reflection coefficient of its antenna between two states in accordance with the data being sent. For further details, refer to ["Tag-to-Interrogator \(T=>R\) communications"](#)

The UCODE 8/8m communicates information by backscatter-modulating the amplitude and/or phase of the RF carrier. Interrogators shall be capable of demodulating either demodulation type.

The encoding format, selected in response to interrogator commands, is either FM0 baseband or Miller-modulated subcarrier.

9.4 Supported commands

The UCODE 8/8m supports all **mandatory** EPCglobal V2.0.1 commands including

- KILL command
- PERMALOCK or LOCK command

In addition the UCODE8/8m supports the following **optional** commands:

- ACCESS
- Block Write (32 bit) on even addresses
- Untraceable

9.5 UCODE 8/8m memory

The UCODE 8/8m memory is implemented according to EPCglobal V2.0.1:

Table 6. UCODE 8 memory sections

Name	Size	Bank
Reserved memory (32-bit Access and 32 bit Kill password)	64 bit	00b
EPC (excluding 16 bit CRC-16 and 16-bit PC)	128 bit	01b
UCODE 8 Configuration Word	16 bit	01b
TID (including permalocked unique 48-bit serial number)	96 bit	10b

Table 7. UCODE 8m memory sections

Name	Size	Bank
Reserved memory (32-bit Access and 32 bit Kill password)	64 bit	00b
EPC (excluding 16 bit CRC-16 and 16-bit PC)	96 bit	01b
UCODE 8 Configuration Word	16 bit	01b
TID (including permalocked unique 48-bit serial number)	96 bit	10b
User Memory	32 bit	11b

The logical address of all memory banks begins at zero (00h).

In addition to the four memory banks, one configuration word to handle the UCODE 8/8m specific features is available at EPC bank 01 address bit-200h. The configuration word is described in detail in [Section 9.6.1](#)

The TID complies to the GS1 EPC Tag Data Standard. See "[EPC Tag Data Standard, Release 1.10](#)"

9.5.1 UCODE 8/8m overall memory map

Table 8. UCODE 8 overall memory map

Bank	Address	Type	Content	Initial	Remark
Bank 00	00h to 1Fh	reserved	Kill password	all 00h	unlocked memory
	20h to 3Fh	reserved	Access password	all 00h	unlocked memory
Bank 01 EPC	00h to 0Fh	EPC	CRC-16: refer to " EPC Global Gen2v2 "		memory mapped calculated CRC
	10h to 14h	EPC	EPC length	00110b	unlocked memory
	15h	EPC	UMI	0b	hardwired to 0
	16h	EPC	XPC indicator	0b	hardwired to 0
	17h to 1Fh	EPC	numbering system indicator	00h	unlocked memory
	20h to 9Fh	EPC	EPC	[1]	unlocked memory
Bank 01 Config Word	200h	EPC	EPC check	0b	indicator bit
	201h	EPC	EPC correction	0b	indicator bit
	202h	EPC	EPC NOK	0b	indicator bit
	203h	EPC	EPC+TID	0b	action bit ^[2]
	204h	EPC	Brand Identifier	0b	action bit ^[2]
	205h	EPC	Self Adjust Cap 1	0b	indicator bit
	206h	EPC	Self Adjust Cap 0	0b	indicator bit
	207h	EPC	Self Adjust disable	0b	permanent bit ^[3]
	208h	EPC	RFU	0b	locked memory
	209h	EPC	max. backscatter strength	1b	permanent bit ^[3]
	20Ah	EPC	RFU	0b	locked memory
	20Bh	EPC	RFU	0b	locked memory
	20Ch	EPC	RFU	0b	locked memory
	20Dh	EPC	RFU	0b	locked memory
	20Eh	EPC	RFU	0b	locked memory
20Fh	EPC	PSF flag	0b	permanent bit ^[3]	
Bank 10 TID	00h to 07h	TID	allocation class identifier	1110 0010b	locked memory
	08h to 13h	TID	tag mask designer identifier	1000 0000 0110b	locked memory
	14h	TID	config word indicator	1b ^[4]	locked memory
	15h to 1Fh	TID	tag model number	TMNR ^[5]	locked memory
	20h to 2Fh	TID	XTID header	2000h	locked memory
	30h to 5Fh	TID	serial number	SNR	locked memory

[1] HEX E280 6894 0000 nnnn nnnn nnnn 0000 0000 where n are the nibbles of the SNR from the TID

[2] Action bits: meant to trigger a feature upon a SELECT command on the related bit ref feature control mechanism, see [Section 9.6.1](#)

[3] Permanent bit: permanently stored bits in the memory; Read/Writeable according to EPC bank lock status, see [Section 9.6.1](#)

[4] Indicates the existence of a Configuration Word at the end of the EPC number

[5] See [Figure 6](#)

Table 9. UCODE 8m overall memory map

Bank	Address	Type	Content	Initial	Remark
Bank 00	00h to 1Fh	reserved	Kill password	all 00h	unlocked memory
	20h to 3Fh	reserved	Access password	all 00h	unlocked memory
Bank 01 EPC	00h to 0Fh	EPC	CRC-16: refer to " EPC Global Gen2v2 "		memory mapped calculated CRC
	10h to 14h	EPC	EPC length	00110b	unlocked memory
	15h	EPC	UMI	1b	hardwired to 1
	16h	EPC	XPC indicator	0b	hardwired to 0
	17h to 1Fh	EPC	numbering system indicator	00h	unlocked memory
	20h to 7Fh	EPC	EPC	[1]	unlocked memory
Bank 01 Config Word	200h	EPC	EPC check	0b	indicator bit
	201h	EPC	EPC correction	0b	indicator bit
	202h	EPC	EPC NOK	0b	indicator bit
	203h	EPC	EPC+TID	0b	action bit ^[2]
	204h	EPC	Brand Identifier	0b	action bit ^[2]
	205h	EPC	Self Adjust Cap 1	0b	indicator bit
	206h	EPC	Self Adjust Cap 0	0b	indicator bit
	207h	EPC	Self Adjust disable	0b	permanent bit ^[3]
	208h	EPC	RFU	0b	locked memory
	209h	EPC	max. backscatter strength	1b	permanent bit ^[3]
	20Ah	EPC	RFU	0b	locked memory
	20Bh	EPC	RFU	0b	locked memory
	20Ch	EPC	User Memory check	0b	indicator bit
	20Dh	EPC	User Memory correction	0b	indicator bit
	20Eh	EPC	User Memory NOK	0b	indicator bit
20Fh	EPC	PSF flag	0b	permanent bit ^[3]	
Bank 10 TID	00h to 07h	TID	allocation class identifier	1110 0010b	locked memory
	08h to 13h	TID	tag mask designer identifier	1000 0000 0110b	locked memory
	14h	TID	config word indicator	1b ^[4]	locked memory
	15h to 1Fh	TID	tag model number	TMNR ^[5]	locked memory
	20h to 2Fh	TID	XTID header	2000h	locked memory
	30h to 5Fh	TID	serial number	SNR	locked memory
Bank 11 User Memory	00h to 1Fh	UM	User Memory	all 00h	unlocked memory

[1] HEX E280 6994 0000 nnnn nnnn nnnn where n are the nibbles of the SNR from the TID

[2] Action bits: meant to trigger a feature upon a SELECT command on the related bit ref feature control mechanism, see [Section 9.6.1](#)

[3] Permanent bit: permanently stored bits in the memory; Read/Writeable according to EPC bank lock status, see [Section 9.6.1](#)

[4] Indicates the existence of a Configuration Word at the end of the EPC number

[5] See [Figure 6](#)

9.5.2 UCODE 8/8m TID memory details

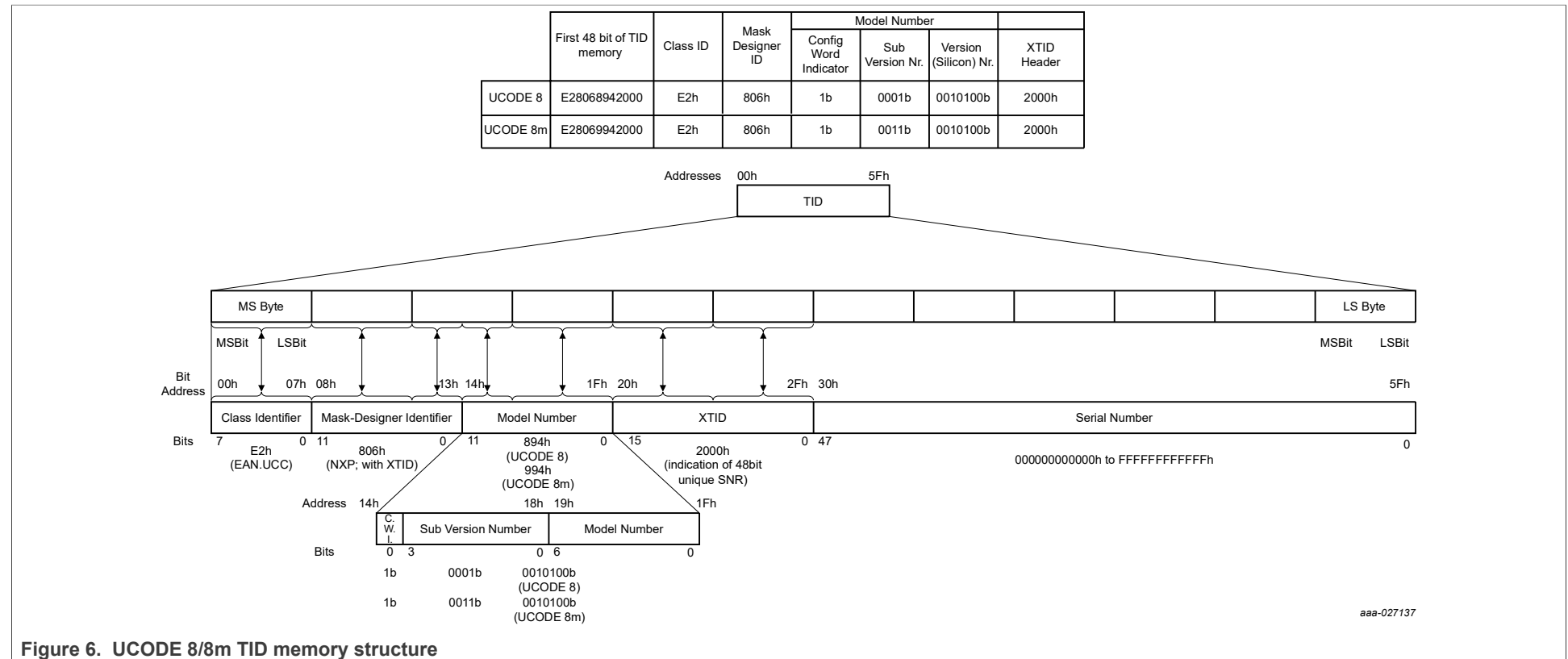


Figure 6. UCODE 8/8m TID memory structure

9.6 Supported features

The UCODE 8/8m is equipped with a number of additional features. They are implemented in such a way that standard EPCglobal READ / WRITE / ACCESS / SELECT commands can be used to operate these features.

The Configuration Word, as mentioned in the memory map, describes the additional features at address 200h of the EPC memory.

Bit 14h of the TID indicates the existence of a Configuration Word. This flag enables the selection of configuration word enhanced transponders in mixed tag populations.

9.6.1 UCODE 8/8m features control mechanism

The different features of the UCODE 8/8m can be activated / de-activated by addressing or changing the content of the corresponding bit in the configuration word at address 200h in the EPC memory bank (see [Table 10](#)). The de-activation of the action bit features will only happen after chip reset.

Table 10. Configuration word UCODE 8/8m

Indicator bit			Action bit		Indicator bit		Permanent bit
EPC Check	EPC Corr	EPC NOK	EPC+TID	Brand Identifier	Self Adjust Cap 1	Self Adjust Cap 0	Self Adjust disable
0	1	2	3	4	5	6	7

Table 11. Configuration word UCODE 8/8m ... continued

Locked memory	Permanent bit	Locked memory		Indicator bit			Permanent bit
RFU	max.backscatter strength	RFU	RFU	User Memory Check	User Memory Corr	User Memory NOK	PSF bit
8	9	10	11	12	13	14	15

The configuration word contains 3 different type of bits:

- **Action bits:** meant to trigger a feature upon a SELECT command on the related bit:
EPC+TID
Brand Identifier
- **Permanent bits:** permanently stored bits in the memory
Self Adjust disable
Max. Backscatter Strength
PSF Alarm bit
- **Indicator bits:** cannot be changed by command
EPC Check/Corr/NOK
User Memory Check/Corr/NOK
Self Adjust Cap0/Cap1

The activation or the de-activation of the feature behind the permanent bits happens only when attempting to write a "1" value to the related bit (value toggling) - writing "0" value has no effect. If the feature is activated, the related bit will be read with a "1" value and, if

de-activated, with a "0" value. The permanent bits can only be toggled by using standard EPC WRITE (not a BlockWrite) if the EPC bank is unlocked or within the SECURED state if the EPC is locked. If the EPC is permalocked, they cannot be changed.

Action bits will trigger a certain action only if the pointer of the SELECT command exactly matches the action-bit address (i.e. 203h or 204h), if the length=1 and if mask=1b (no multiple triggers of actions possible within one single SELECT command).

If the truncate bit in the SELECT command is set to "1", the SELECT will be ignored. A SELECT on action bits will not change the digital state of the chip.

The action bits can be triggered regardless if the EPC memory is unlocked, locked or permalocked.

9.6.2 Memory Safeguard

9.6.2.1 Description

The Memory Safeguard of UCODE 8/8m consist of three different countermeasures which ensure integrity of the stored data:

ECC (Error correction code):

The implemented ECC is applied on the EPC- and User-Memory. With this feature, a single bit failure in the memory is detected and corrected automatically. In case of 2 bit fail, an indication is given.

EPC Memory:

The config word bit 200h (EPC check) indicates, if the EPC check is active ("1"). In case a single bit was corrected this will be indicated by the bit 201h (EPC Corr). Should a 2-bit failure occur bit 202h (EPC NOK) will be activated ("1"). In this case, no error correction will be applied and the EPC memory content readout will provide the actual content.

User Memory:

The config word bit 20Ch (User Memory check) indicates if the User Memory check is active ("1"). In case a single bit was corrected this will be indicated by the bit 20Dh (User Memory Corr). Should a 2-bit failure occur, bit 20Eh (User Memory NOK) will be activated ("1"). In this case, no error correction will be applied and the User Memory content readout will provide the actual content.

This feature will be activated in case a Lock operation is applied on the according memory bank. If there is a password lock and a change of the memory content in the secured state, the ECC will be not re-calculated and the feature is disabled. To re-enable the ECC functionality also in this condition, an unlock and re-lock is required.

Parity check:

A parity check on the TID is implemented to offer the possibility to identify a change in the TID. The parity bit (Even parity) will be calculated and locked in the manufacturing process. For a check, the TID content needs to be read out and parity checked.

Margin Check

The implemented margin check is acting on the EPC-, Reserved- and User-Memory. During performing a Lock operation on the targeted memory bank the IC checks for sufficient programming margin of the memory cell and only responds after a successful check. In case of insufficient margin an error code will be responded and the Lock not completed. A re-check on already locked memory banks requires an unlock and re-lock command.

9.6.3 Self Adjust

9.6.3.1 Description

The UCODE 8/8m has an automatic mechanism implemented which adjusts the chip sensitivity to a maximum in the operated environment. This adjustment will be performed at startup and selects between three different input capacitance values. The feature is enabled by default, but can also be deactivated by the config word bit 207h (Self Adjust disable). In case of deactivation, the center capacitance is used.

The indicator bits 205h (Self Adjust Cap 1) and 206h (Self Adjust Cap 0) give information which capacitor is active ("1"). The startup is performed with the lowest value which is center capacitance minus Cap 0 (60 fF) and is then adjusted up to center capacitance plus Cap 1 (100 fF).

9.6.4 Brand Identifier

9.6.4.1 Description

This new feature allows brand owners to implement a product originality check option for their products. The customer dedicated unique 16-bit brand identifier is programmed during manufacturing process by NXP and therefore unalterable stored in the memory.

A SELECT command on bit 204h (Brand identifier) in the configuration word triggers the UCODE8/8m to respond in the inventory round with PC + EPC + Brand Identifier + CRC. In order to prevent manipulation, the Brand Identifier is scrambled with the RN16 and not sent in plain. The implemented scrambling is performed by bitwise XOR operation of the 16-bit Brand Identifier and the RN16. At the reader, the Brand identifier can be descrambled and the originality check completed.

The PC value is adjusted accordingly for UCODE 8/8m. A SELECT on the Brand Identifier bit always gives a Tag matching.

The usage of this feature requires an update on the reader firmware with the Brand Identifier check routine.

Default value of the UCODE 8/8m Brand Identifier is "AAAAh". Customer-specific Brand Identifiers can be requested by a dedicated product ordering code. For details, contact your NXP sales representative.

The Brand Identifier feature cannot be used in combination with the EPC+TID feature.

9.6.5 EPC+TID

9.6.5.1 Description

This feature enables the read out the EPC+TID memory content in a faster way compared to a standard readout sequence.

A SELECT on the config word bit 203h (EPC+TID) will trigger the UCODE 8/8m to reply with the EPC+TID after receiving the ACK command during the inventory round.

In case only the TID should be replied by this feature, the EPC length in the PC needs to be set to "0".

9.6.6 Product Status Flag (PSF)

9.6.6.1 Description

The PSF bit can be used for easy EAS (Electronic Article Surveillance) implementations or as general-purpose check flag.

In order to detect tags with activated PSF, a SELECT command on bit 20Fh (PSF Bit) in the configuration word is required. In the following inventory round, only PSF enabled chips reply their EPC number.

9.6.7 Backscatter strength reduction

The UCODE 8/8m features two levels of backscatter strengths. Per default, maximum backscatter is enabled in order to enable maximum read rates. A deactivation of this feature can be done by clearing bit 209h (max. backscatter strength) in the configuration word, which reduces the backscatter strength if needed.

9.6.8 Pre-serialization of the 96-bit EPC

9.6.8.1 Description

UCODE 8/8m are delivered with a pre-serialized content of the 96-bit EPC, which is the initial EPC length settings of UCODE 8/8m.

The EPC content is identical to the TID content except of the 16-bit XTID content which is set to 16-bit 0's.

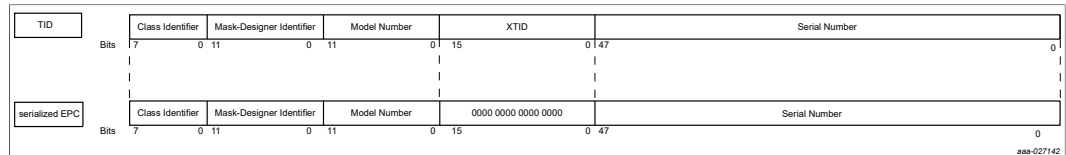


Figure 7. Pre-serialization of 96-bit EPC

9.6.9 Single-slit antenna solution

9.6.9.1 Description

In UCODE 8/8m, the test pads TP1 and TP2 are electrically disconnected and therefore can be safely short-circuited to the RF pads (RF1, RF2) (see figure below).

Single-slit antenna enables easier assembly and antenna design. In addition to the standard antenna assembly, the related increased input capacitance (see [Table 15](#)) can be used for optimization for different antenna design.

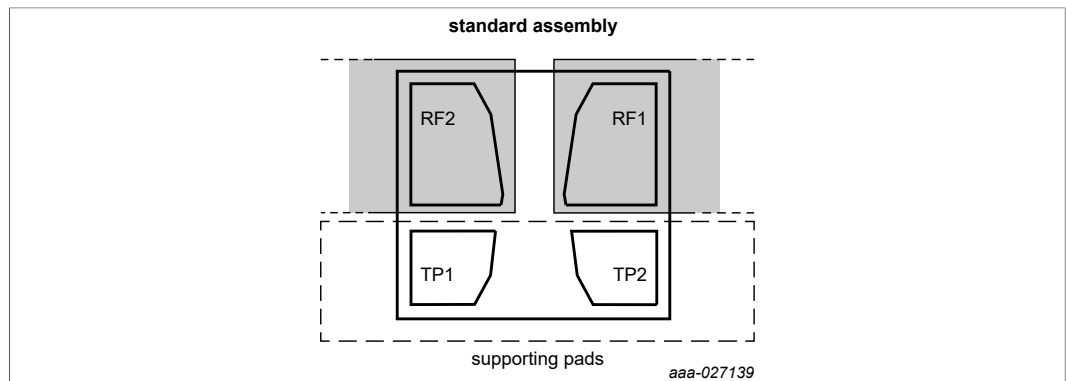


Figure 8. Standard antenna design versus single-slit antenna

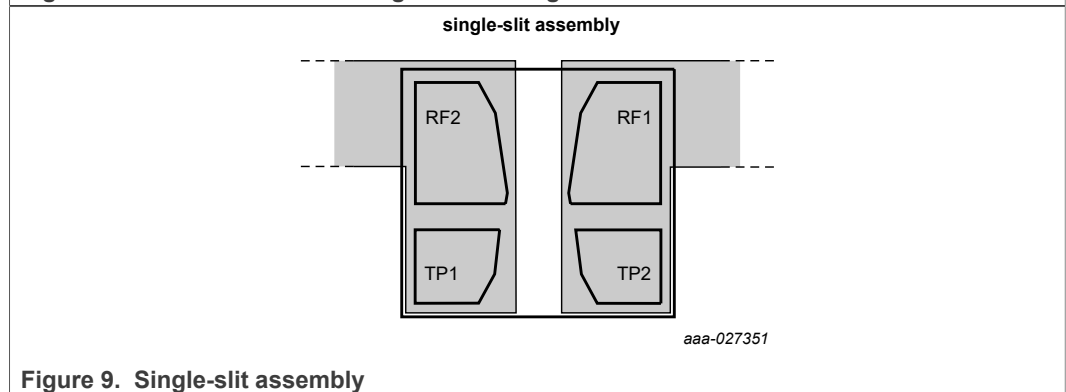


Figure 9. Single-slit assembly

9.6.10 Large Pads

9.6.10.1 Description

The large gold pads introduced in UCODE 8/8m enable more robust and reliable assembly. The new pad design allows not only more freedom in the placement accuracy (see ["Rotation tolerant pad design"](#)). It also brings advantages in high-speed assembly due to the dual axis glue spacer (see ["Dual axis glue spacer"](#)).

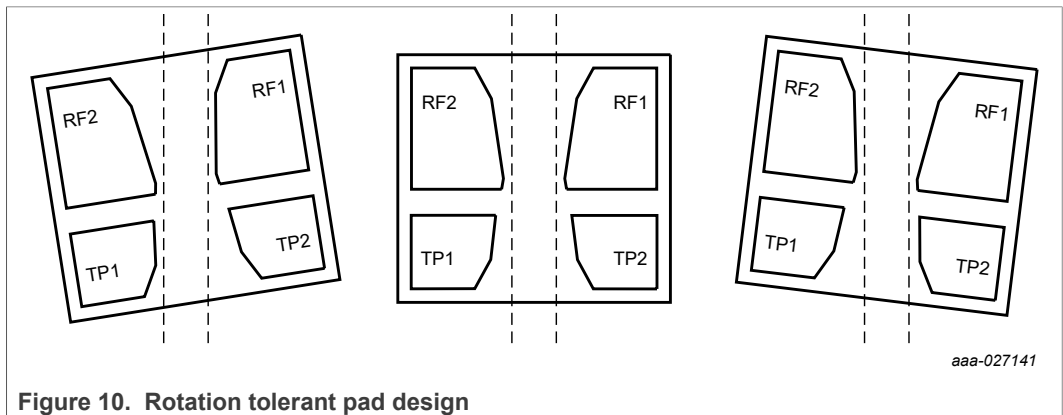


Figure 10. Rotation tolerant pad design

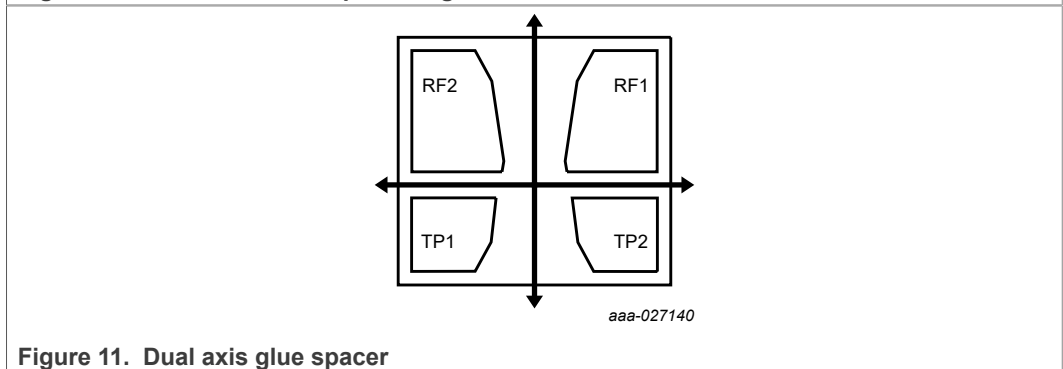


Figure 11. Dual axis glue spacer

9.6.11 Custom commands

The Untraceable function allows the UCODE 8/8m to hide the complete or parts of the EPC, TID and/or user memory. In addition, the read range can be completely or temporarily reduced. This command can only be executed from the secured state. Memory parts which are set untraceable are acting as non-existing in the Open state.

EPC-field: Specifies the number of words of the EPC memory which the UCODE 8/8m back scatters. A change of this field therefore also changes the L bit in the Protocol Control (PC) word.

TID-field: Hide some ("01") hides the TID memory from address 20h (included) onwards.

Range-field: In case of activated range toggling, the read range reduction toggles from the actual value to the second (e.g. when actual state is normal it toggles to reduced). In case of power loss the chip reverts to its prior state.

UCODE 8/8m does not support the U bit and therefore ignores this value.

Table 12. Untraceable command

	Command	RFU	U	EPC	TID	User	Range	RN	CRC
No. of bits	16	2	1	6	2	1	2	16	16
Description	1110 0010 0000 0000	00	do not care	MSB:"0": show memory above EPC "1": hide memory above EPC 5 LSBs: new EPC length	"00": hide none "01": hide some "10": hide all "11": RFU	"0": view "1": hide	"00": normal "01": toggle "10": reduced "11": RFU	handle	CRC-16

Table 13. Untraceable command-response table

Starting State	Condition	Response	Next State
ready	all	-	ready
arbitrate, reply, acknowledged	all	-	arbitrate
open	all	-	open
secured	executable	backscatter header when done	secured
killed	all	-	killed

In case of access to the memory that is set to untraceable, the error condition "memory overrun" is returned.

For further details, refer to ["EPC Global Gen2v2"](#)

10 Limiting values

Table 14. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to RFN. ^{[1] [2]}

Symbol	Parameter	Conditions	Min	Max	Unit
Bare die limitations					
T _{stg}	storage temperature		-55	+125	°C
T _{amb}	ambient temperature		-40	+85	°C
V _{ESD}	electrostatic discharge voltage	Human body model ^{[3] [4]}	-	± 2	kV
Pad limitations					
P _i	input power	maximum power dissipation, RF1/RF2 pad	-	100	mW

- [1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the Operating Conditions and Electrical Characteristics section of this specification is not implied.
- [2] This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
- [3] For ESD measurement, the die chip has been mounted into a CDIP20 package.
- [4] HBM: ANSI/ESDA/JEDEC JS-001

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

11 Characteristics

11.1 UCODE 8/8m bare die characteristics

Table 15. UCODE 8/8m RF interface characteristics (RF1, RF2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_i	input frequency		840	-	960	MHz
$P_{I(min)}$	minimum input power	READ sensitivity	[1] [2] [3]	- 22.9	-	dBm
		reduced operating range	[4]	+ 1	-	dBm
$P_{I(min)}$	minimum input power	WRITE sensitivity	[4]	-17.8	-	dBm
t_{16bit}	encoding speed	16-bit	[5]	0.7	-	ms
		32-bit (block write)	[5]	1.2	-	ms
C_i	chip input capacitance, Large Pads	parallel	[2] [6] [7]	0.69	-	pF
Z	chip impedance, Large Pads	866 MHz	[2] [6] [7]	15-j265	-	Ω
		915 MHz	[2] [6] [7]	14-j252	-	Ω
		953 MHz	[2] [6] [7]	13-j242	-	Ω
Z	typical assembled impedance, Large Pads (see Figure 8)	915 MHz	[8] [9] [7]	19-j234	-	Ω
Z	typical assembled impedance in case of single-slit antenna assembly, Large Pads (see Figure 9)	915 MHz	[8] [10] [7]	13-j191	-	Ω

- [1] Power to process a QUERY command
- [2] Measured with a 50 Ω source impedance directly on the chip
- [3] Results in approximately -23 dBm tag sensitivity with a 2.15 dBi gain antenna
- [4] Tag sensitivity on a 2.15 dBi gain antenna
- [5] When the memory content is "0000...".
- [6] At minimum operating power
- [7] at center capacitor of Self Adjust
- [8] The antenna shall be matched to this impedance
- [9] Assuming 50ff additional assembly capacitance
- [10] Assuming 220ff additional assembly+test pad capacitance

Table 16. UCODE 8/8m memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
EEPROM characteristics						
t_{ret}	retention time	$T_{amb} \leq 55 \text{ }^\circ\text{C}$	20	-	-	year
$N_{endu(W)}$	write endurance		100k	-	-	cycle

12 Packing information

12.1 Wafer

See ["Data sheet - Delivery type description – General specification for 8" wafer on UV-tape with electronic fail die marking, BU-S&C document number: 1093**"](#)

See ["Data sheet - Delivery type description – General specification for 12" wafer on UV-tape with electronic fail die marking, BU-S&C document number: 1862**"](#)

13 Abbreviations

Table 17. Abbreviations

Acronym	Description
CRC	Cyclic Redundancy Check
CW	Continuous Wave
DSB-ASK	Double Side Band-Amplitude Shift Keying
DC	Direct Current
EAS	Electronic Article Surveillance
EEPROM	Electrically Erasable Programmable Read Only Memory
EPC	Electronic Product Code (containing Header, Domain Manager, Object Class and Serial Number)
FM0	Bi phase space modulation
G2	Generation 2
IC	Integrated Circuit
PIE	Pulse Interval Encoding
PSF	Product Status Flag
RF	Radio Frequency
UHF	Ultra High Frequency
SECS	Semi Equipment Communication Standard
TID	Tag IDentifier

14 References

1. EPCglobal: EPC Radio-Frequency Identity Protocols Class-1 Generation-2 UHF RFID Protocol for Communications at 860 MHz – 960 MHz, Version 2.0.1 (April 2015)
2. EPCglobal: EPC Tag Data Standard, Release 1.10 (March 2017)
3. Data sheet - Delivery type description – General specification for 8" wafer on UV-tape with electronic fail die marking, BU-S&C document number: 1093**
4. Data sheet - Delivery type description – General specification for 12" wafer on UV-tape with electronic fail die marking, BU-S&C document number: 1862**¹

¹ ** ... document version number

15 Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SL3S1205_15 v. 3.5	20210401	Product data sheet	-	SL3S1205_15 v. 3.4
Modifications:	<ul style="list-style-type: none"> • Table 1 "Ordering information": Ordering information with UCODE 8, 12 inch plasma dicing updated • Section 7 "Wafer layout": Titles in wafer layout with stealth dicing and conventional dicing updated • Figure 5 "UCODE 8/8m, 12" wafer layout, Large Pads, plasma dicing": inserted • Table 5 "12 inch specification with Large Pads, plasma dicing ": inserted • Delivery form of UCODE 8/8m, 12 inch FC Bumps (SL3S1205FUD2/KP and SL3S1215FUD2/KP) discontinued • Related information removed 			
SL3S1205_15 v. 3.4	20200131	Product data sheet	-	SL3S1205_15 v. 3.3
Modifications:	<ul style="list-style-type: none"> • Introduction of 12 inch FC Bumps 			
SL3S1205_15 v. 3.3	20191028	Product data sheet	-	SL3S1205_15 v. 3.2
Modifications:	<ul style="list-style-type: none"> • Section 8.1.2 "12 inch Wafer with Large Pads": number of PGDW changed into 258934 			
SL3S1205_15 v. 3.2	20181119	Product data sheet	-	SL3S1205_15 v. 3.1
Modifications:	<ul style="list-style-type: none"> • Introduction of 12 inch wafer delivery • Figure 3 "UCODE 8/8m, 8" wafer layout, Large Pads, stealth dicing" updated • Editorial changes in Table 8 "UCODE 8 overall memory map" • Editorial changes in Table 9 "UCODE 8m overall memory map" • Section 9.6.4 "Brand Identifier" updated 			
SL3S1205_15 v. 3.1	20170630	Product data sheet	-	SL3S1205_15 v. 3.0
Modifications:	<ul style="list-style-type: none"> • Wording: "Auto Adjust" replaced with "Self Adjust" 			
SL3S1205_15 v. 3.0	20170703	Product data sheet	-	398420
398420	20170531	Preliminary data sheet	-	398410
398410	20160919	Objective data sheet	-	-

16 Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

16.2 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

16.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without

notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications. In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified or documented vulnerabilities. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

UCODE — is a trademark of NXP B.V.

NXP — wordmark and logo are trademarks of NXP B.V.

Tables

Tab. 1.	Ordering information	5	Tab. 10.	Configuration word UCODE 8/8m	20
Tab. 2.	Pin description bare die	7	Tab. 11.	Configuration word UCODE 8/8m ... continued	20
Tab. 3.	8 inch specification with Large Pads, stealth dicing	11	Tab. 12.	Untraceable command	27
Tab. 4.	12 inch specification with Large Pads, conventional dicing	12	Tab. 13.	Untraceable command-response table	27
Tab. 5.	12 inch specification with Large Pads, plasma dicing	13	Tab. 14.	Limiting values	28
Tab. 6.	UCODE 8 memory sections	16	Tab. 15.	UCODE 8/8m RF interface characteristics (RF1, RF2)	29
Tab. 7.	UCODE 8m memory sections	16	Tab. 16.	UCODE 8/8m memory characteristics	29
Tab. 8.	UCODE 8 overall memory map	17	Tab. 17.	Abbreviations	31
Tab. 9.	UCODE 8m overall memory map	18	Tab. 18.	Revision history	33

Figures

Fig. 1.	Block diagram of UCODE 8/8m IC	6	Fig. 6.	UCODE 8/8m TID memory structure	19
Fig. 2.	Pinning bare die, Large Pads	7	Fig. 7.	Pre-serialization of 96-bit EPC	24
Fig. 3.	UCODE 8/8m, 8" wafer layout, Large Pads, stealth dicing	8	Fig. 8.	Standard antenna design versus single-slit antenna	25
Fig. 4.	UCODE 8/8m, 12" wafer layout, Large Pads, conventional dicing	9	Fig. 9.	Single-slit assembly	25
Fig. 5.	UCODE 8/8m, 12" wafer layout, Large Pads, plasma dicing	10	Fig. 10.	Rotation tolerant pad design	26
			Fig. 11.	Dual axis glue spacer	26

Contents

1	General description	1	12.1	Wafer	30
2	Features and benefits	2	13	Abbreviations	31
2.1	Key features	2	14	References	32
2.1.1	Memory	2	15	Revision history	33
2.2	Supported features	3	16	Legal information	34
3	Applications	4			
3.1	Target market	4			
3.2	Applications	4			
4	Ordering information	5			
5	Block diagram	6			
6	Pinning information	7			
6.1	Pin description	7			
7	Wafer layout	8			
8	Mechanical specification	11			
8.1	Wafer specification	11			
8.1.1	8 inch Wafer with Large Pads, stealth dicing	11			
8.1.2	12 inch Wafer with Large Pads	12			
8.1.3	Fail die identification	14			
8.1.4	Map file distribution	14			
9	Functional description	15			
9.1	Air interface standards	15			
9.2	Power transfer	15			
9.3	Data transfer	15			
9.3.1	Interrogator to tag Link	15			
9.3.2	Tag to interrogator Link	15			
9.4	Supported commands	16			
9.5	UCODE 8/8m memory	16			
9.5.1	UCODE 8/8m overall memory map	17			
9.5.2	UCODE 8/8m TID memory details	19			
9.6	Supported features	20			
9.6.1	UCODE 8/8m features control mechanism	20			
9.6.2	Memory Safeguard	22			
9.6.2.1	Description	22			
9.6.3	Self Adjust	23			
9.6.3.1	Description	23			
9.6.4	Brand Identifier	23			
9.6.4.1	Description	23			
9.6.5	EPC+TID	24			
9.6.5.1	Description	24			
9.6.6	Product Status Flag (PSF)	24			
9.6.6.1	Description	24			
9.6.7	Backscatter strength reduction	24			
9.6.8	Pre-serialization of the 96-bit EPC	24			
9.6.8.1	Description	24			
9.6.9	Single-slit antenna solution	25			
9.6.9.1	Description	25			
9.6.10	Large Pads	26			
9.6.10.1	Description	26			
9.6.11	Custom commands	27			
10	Limiting values	28			
11	Characteristics	29			
11.1	UCODE 8/8m bare die characteristics	29			
12	Packing information	30			

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2021.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 1 April 2021
Document number: 398435