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MT6762-SBS

MODEM

[20] DVDD_MODEM_6357_FB[6]
[20] DVDD_MODEM_6357_GND[6]

DVDD_MODEM

R9	DVDD_VDD_MODEM
T10	DVDD_VDD_MODEM
U9	DVDD_VDD_MODEM
U13	DVDD_VDD_MODEM
V10	DVDD_VDD_MODEM
V13	DVDD_VDD_MODEM
W9	DVDD_VDD_MODEM
W10	DVDD_VDD_MODEM
W8	DVDD_VDD_MODEM
Y8	DVDD_VDD_MODEM

SH101 SHORT / 4MIL
SH102 SHORT / 4MIL

C101 22uF
C102 22uF
C103 1uF
C104 1uF
C105 1uF
C106 1uF

D_GND

GPU

DVDD_CORE

DVDD_MFGSYS	K20
DVDD_MFGSYS	L19
DVDD_MFGSYS	L20
DVDD_MFGSYS	M20
DVDD_MFGSYS	N19
DVDD_MFGSYS	N20
DVDD_MFGSYS	P20
DVDD_MFGSYS	T20
DVDD_MFGSYS	T21

C145 22uF
C144 1uF
C143 1uF
C142 1uF
C141 1uF

D_GND

CPU

DVDD_DVFS

DVDD_DVFS	U16
DVDD_DVFS	U18
DVDD_DVFS	U20
DVDD_DVFS	U22
DVDD_DVFS	Y16
DVDD_DVFS	Y18
DVDD_DVFS	Y20
DVDD_DVFS	Y21
DVDD_DVFS	Y22
DVDD_DVFS	AA16
DVDD_DVFS	AA18
DVDD_DVFS	AA20
DVDD_DVFS	AA21
DVDD_DVFS	AA22
DVDD_DVFS	AB16
DVDD_DVFS	AB18

DVDD_DVFS_6357_FB [6]
DVDD_DVFS_6357_GND [6]

SH105 SHORT / 4MIL
SH106 SHORT / 4MIL

C140 22uF
C139 22uF
C138 1uF
C137 1uF
C136 1uF
C135 1uF
C134 2.2uF
C133 2.2uF

D_GND

OPT_MARK 1 OPT1
OPT_MARK 1 OPT2
OPT_MARK 1 OPT3
OPT_MARK 1 OPT4

SRAM

VSRAM_OTHERS_PMU

C107 470nF → R19 DVDD_MFG_SRAM

D_GND

VSRAM_OTHERS_PMU

C108 470nF → L13 DVDD_TOP_SRAM
C109 470nF → V12 DVDD_TOP_SRAM

D_GND

DVDD_SRAM_DVFS

C110 1uF → V15 DVDD_MCUSYS_SRAM

D_GND

CORE

DVDD_CORE

DVDD_TOP	J21
DVDD_TOP	K10
DVDD_TOP	K13
DVDD_TOP	K14
DVDD_TOP	K17
DVDD_TOP	L17
DVDD_TOP	M10
DVDD_TOP	M14
DVDD_TOP	M18
DVDD_TOP	N13
DVDD_TOP	N17
DVDD_TOP	P10
DVDD_TOP	P13
DVDD_TOP	P14
DVDD_TOP	P18
DVDD_TOP	P23
DVDD_TOP	R13
DVDD_TOP	R17
DVDD_TOP	T18

DVDD_CORE_6357_FB [6] [20]
DVDD_CORE_6357_GND [6] [20]

SH103 SHORT / 4MIL
SH104 SHORT / 4MIL

C132 22uF
C131 22uF
C130 1uF
C129 1uF
C128 1uF
C127 1uF
C126 1uF
C125 1uF
C124 1uF
C123 1uF
C122 1uF
C121 1uF

D_GND

VDDQ

VDRAM_PMU

C112	100nF	H11 AVDDQ_EMI0
C113	100nF	H12 AVDDQ_EMI0
C114	100nF	H18 AVDDQ_EMI1
C115	100nF	H19 AVDDQ_EMI1
C116	2.2uF	H10 AVDD2_EMI
C117	4.7uF	H13 AVDD2_EMI
C118	10uF	H17 AVDD2_EMI
		H20 AVDD2_EMI

D_GND

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GND

A11 DVSS
A13 DVSS
A15 DVSS
B3 DVSS
B21 DVSS
C2 DVSS
C6 DVSS
C12 DVSS
C16 DVSS
C20 DVSS
C23 DVSS
D3 DVSS
D9 DVSS
D13 DVSS
D23 DVSS
D27 DVSS
E4 DVSS
E24 DVSS
E25 DVSS
F2 DVSS
F4 DVSS
F5 DVSS
F6 DVSS
F7 DVSS
F8 DVSS
F10 DVSS
F11 DVSS
F12 DVSS
F14 DVSS
F17 DVSS
F19 DVSS
F20 DVSS
F21 DVSS
F22 DVSS
F23 DVSS
G4 DVSS
G6 DVSS
G11 DVSS
G12 DVSS
G13 DVSS
G14 DVSS
G15 DVSS
G21 DVSS
G22 DVSS
G26 DVSS
H14 DVSS
H15 DVSS
H22 DVSS
H25 DVSS
J22 DVSS
J23 DVSS
J24 DVSS
K9 DVSS
K11 DVSS
K12 DVSS
K15 DVSS
K16 DVSS
K18 DVSS
L8 DVSS
L11 DVSS
L15 DVSS
L16 DVSS
L21 DVSS
L22 DVSS
L26 DVSS
M6 DVSS
M7 DVSS
M12 DVSS
M16 DVSS
M22 DVSS
M24 DVSS
M28 DVSS
N6 DVSS
N7 DVSS
N11 DVSS
N15 DVSS
N21 DVSS
N22 DVSS
P7 DVSS
P12 DVSS
P16 DVSS
P21 DVSS
P22 DVSS
R11 DVSS
R15 DVSS
R21 DVSS
R22 DVSS
T8 DVSS
T12 DVSS
T22 DVSS
U11 DVSS
V8 DVSS
V16 DVSS
V17 DVSS
V19 DVSS
V21 DVSS
W17 DVSS
W19 DVSS
W21 DVSS
AA9 DVSS
AA11 DVSS
AA13 DVSS
AB10 DVSS
AB12 DVSS
AD7 DVSS
AD11 DVSS
AD14 DVSS
AE8 DVSS
AE11 DVSS
AE14 DVSS
AF8 DVSS
AF11 DVSS
AF14 DVSS
AF17 DVSS
AF28 DVSS
AG26 DVSS

D_GND

AVDD & MD_A

AVDD12_MD AG21
AVDD18_MD AG19
AVDD18_AP AG18
AVDD18_CPU AC18

VA12_PMU
C201 100nF D_GND

AVDD18_SOC
AVDD18_SOC
AVDD18_SOC
C202 1uF D_GND
C203 1uF D_GND
C204 1uF D_GND

PLL

AVDD18_DDR H21
EMI_VDD1
C205 100nF D_GND
C206 1uF D_GND

AVDD12_PLLGP T14
VA12_PMU
AVDD18_PLLGP T16
AVDD18_SOC
C207 100nF D_GND
C208 100nF D_GND

PERI_D

DVDD18_IOLT G28
DVDD18_IOLM W28
DVDD18_IOBL AG27
DVDD18_IORB U1
DVDD18_IORB AG6
DVDD18_IORT J1
VIO18_PMU
C209 100nF/NC D_GND
C210 100nF D_GND
C211 100nF/NC D_GND
C212 100nF D_GND
C213 100nF D_GND

DVDD_VQPS AD18
VEFUSE_PMU

DVDD18_MSDC0 A27

DVDD28_MSDC1 AD28
VMC_PMU

DVDD28_SIM1 AE28
VSIM1_PMU

DVDD28_SIM2 AC28
VSIM2_PMU

DVDD18_MSDC1 AA28
DVDD18_SIM AB28
C214 100nF D_GND
C215 1uF D_GND
C216 100nF D_GND
C217 100nF D_GND
Note: 11-1
Note: 11-2

C218 100nF D_GND
C219 100nF D_GND
Note: 11-3

PERI_A

AVDD12_CSI U2
VA12_PMU
AVDD12_DSI R28
VA12_PMU
C220 1uF D_GND
C221 1uF D_GND

AVDD04_DSI T28
DVDD_CORE
C222 1uF D_GND

AVDD18_USB D28
AVDD18_SOC
AVDD12_USB E28
VA12_PMU
AVDD33_USB B28
VUSB_PMU
C223 1uF D_GND
C224 100nF D_GND
C225 1uF D_GND

AVDD18_WBG H2
AVDD18_SOC
AVDD12_WBG C3
VA12_PMU
C227 100nF D_GND
C226 100nF D_GND

Schematic design notice of "11_BB_POWER_IO" page.

Note 11-1: C4101 closed DVDD18_MSDC0 150mil

Note 11-2: C4302 closed DVDD28_MSDC1 150mil

Note 11-3: C4301 closed DVDD18_MSDC1 150mil

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PMU_IF

[8]	SYSRSTB	E27	SYSRSTB
[8,10]	WATCHDOG	K24	WATCHDOG
[8]	SRCLKENA0	L25	SRCLKENA0
[8,13]	SRCLKENA1	M25	SRCLKENA1
[8]	RTC32K_CK	H26	RTC32K_CK
[3,8]	PWRAP_SPI0_CSN	K27	PWRAP_SPI0_CSN
[8]	PWRAP_SPI0_CK	L27	PWRAP_SPI0_CK
[3,8]	PWRAP_SPI0_MO	M27	PWRAP_SPI0_MO
[3,8]	PWRAP_SPI0_MI	K28	PWRAP_SPI0_MI
[9]	AUD_CLK_MOSI	J25	AUD_CLK_MOSI
[9]	AUD_CLK_MISO	G27	AUD_CLK_MISO
[9]	AUD_DAT_MISO0	J27	AUD_DAT_MISO0
[9]	AUD_DAT_MISO1	J28	AUD_DAT_MISO1
[3,9]	AUD_DAT_MOSI0	K26	AUD_DAT_MOSI0
[9]	AUD_DAT_MOSI1	K25	AUD_DAT_MOSI1
[9]	AUD_SYNC_MISO	H27	AUD_SYNC_MISO
[9]	AUD_SYNC_MOSI	J26	AUD_SYNC_MOSI

Test Pin

F27	TESTMODE	
W13	TP_PLLGP	
W12	TN_PLLGP	
AC5	CDM3P5A	
AB6	CDM5P5A	

D_GND

A1	NC	
A28	NC	
AG1	NC	
AG28	NC	

VIO18_PMU
R306
390K 1%
[3] AUX_IN1_NTC
AUX_IN1_NTC
NTC302
NCP15WF104F03RC
D_GND

Thermistor to sense RF PA temperature

1. NTC302 must close to LTE Band 7 PA or the hottest PA <2mm.
2. **The distance is the shortest distance from package edge to edge.**

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MT6762-SBS

SIM

[18]	SIM1_SCLK	AA25	SIM1_SCLK
[18]	SIM1_SIO	Y25	SIM1_SIO
[18]	SIM1_SRST	AA26	SIM1_SRST
[18]	SIM2_SCLK	AC25	SIM2_SCLK
[18]	SIM2_SIO	AB25	SIM2_SIO
[18]	SIM2_SRST	AC26	SIM2_SRST

RFIC_Ctrl

[13]	RFIC0_BSI_EN	AE21	RFIC0_BSI_EN
[13]	RFIC0_BSI_CK	AF22	RFIC0_BSI_CK
[13]	RFIC0_BSI_D0	AE20	RFIC0_BSI_D0
[13]	RFIC0_BSI_D1	AF21	RFIC0_BSI_D1
		AG22	RFIC0_BSI_D2

RF MIPI

[15]	MIPI0_SCLK	AG7	MISC_BSI_CK_0
[15]	MIPI0_SDATA	AF7	MISC_BSI_DO_0
[14]	MIPI1_SCLK	AF5	MISC_BSI_CK_1
[14]	MIPI1_SDATA	AF6	MISC_BSI_DO_1
		AE6	MISC_BSI_CK_2
		AD6	MISC_BSI_DO_2
	MIPI3_SCLK	AE5	MISC_BSI_CK_3
	MIPI3_SDATA	AD5	MISC_BSI_DO_3

BPI

		AE2	BPI_PA_VM1
		AD3	BPI_PA_VM0
		AF24	BPI_BUS15_ANT2
		AE3	BPI_BUS14_ANT1
		AE25	BPI_BUS13_ANT0
		AE24	BPI_BUS12_OLAT1
		AD4	BPI_BUS11_OLAT0
		AF25	BPI_BUS10
[21]	BPI_BUS9	AF26	BPI_BUS9
	BPI_BUS8	AD25	BPI_BUS8
[21]	BPI_BUS7	AC6	BPI_BUS7
[16]	BPI_BUS6	AG4	BPI_BUS6
[16]	BPI_BUS5	AG3	BPI_BUS5
[16]	BPI_BUS4	AG2	BPI_BUS4
		AF4	BPI_BUS3
	BPI_BUS2	AF3	BPI_BUS2
		AF2	BPI_BUS1
[16]	BPI_BUS0	AE4	BPI_BUS0

ABB_IF

MAIN_X26M_IN	AB13		PMIC_CLK_BB	[8]
TX_BB_IP0	AE9		LTE_TX_BB_IP0	[13]
TX_BB_IN0	AD9		LTE_TX_BB_IN0	[13]
TX_BB_QP0	AE10		LTE_TX_BB_QP0	[13]
TX_BB_QN0	AD10		LTE_TX_BB_QN0	[13]
PRX_BB_I0P	AE13	6177_i0 6177m_iP	LTE_PRX_BB_I0	[13]
PRX_BB_I0N	AG13	6177m_iN		
PRX_BB_I1	AF15	6177_i1	LTE_PRX_BB_I1	[13]
PRX_BB_Q0P	AF12	6177_q0 6177m_qP	LTE_PRX_BB_Q0	[13]
PRX_BB_Q0N	AG12	6177m_qN		
PRX_BB_Q1	AG15	6177_q1	LTE_PRX_BB_Q1	[13]
DRX_BB_I0P	AD13	6177_i0 6177m_iP	LTE_DRX_BB_I0	[13]
DRX_BB_I0N	AE13	6177m_iN		
DRX_BB_I1	AG16	6177_i1	LTE_DRX_BB_I1	[13]
DRX_BB_Q0P	AD12	6177_q0 6177m_qP	LTE_DRX_BB_Q0	[13]
DRX_BB_Q0N	AE12	6177m_qN		
DRX_BB_Q1	AF16	6177_q1	LTE_DRX_BB_Q1	[13]
DET_IP0	AG9		LTE_DET_BB_IP0	[13]
DET_IN0	AF9		LTE_DET_BB_IN0	[13]
DET_QP0	AF10		LTE_DET_BB_QP0	[13]
DET_QN0	AG10		LTE_DET_BB_QN0	[13]
RFIC_ET0_P	AD8			
RFIC_ET0_N	AC9			
APC	AC10		APC1	[15]

Note: 12-5

AUX IN

AUXIN4	AE17	D_GND	
AUXIN3	AE18	ID_FINGER	[23]
AUXIN2	AE19	LCD_ID	
AUXIN1	AF19	AUX_IN1_NTC	[3]
AUXIN0	AF20	AUX_IN0_NTC	[3]

C302 1uF D_GND
C303 1uF D_GND
C304 0
C305 1uF

Note: 12-2

REF POWER

REFP AF18 REFP
C301 100nF D_GND

Note: 12-1

VIO18_PMU
R301
12 K / NC
[3,9] AUD_DAT_MOSI0
[3,8] PWRAP_SPI0_CSN
R302
12K / NC
D_GND

Note: 12-3

VIO18_PMU
R303
NC
[3,8] PWRAP_SPI0_MO
[3,8] PWRAP_SPI0_MI
R304
12K
D_GND

Note: 12-4

VIO18_PMU
R305
390K 1%
AUX_IN0_NTC [3]
NTC301
NCP15WF104F03RC
D_GND

Thermistor to sense AP temperature

1. NTC301 must keep a distance about 6~8 mm away from AP and far from other heat sources 10 mm at least.
2. The distance is the shortest distance from package edge to edge.

Schematic design notice of "12_BB_1" page.

Note 12-1: The de-coupling cap. for REFP (AF18 ball) have to be placed as close to BB as possible.

Note 12-2: To shunt a 1uF capacitor in the AUXIN ADC input to prevent noise coupling. It should be placed as close to BB as possible. Connect the unused AUX ADC input to GND.

Note 12-3: "PWRAP_SPI0_CSN" and "AUD_DAT_MOSI0" are bootstrap pin to select which interface will be the JTAG pin out.

PWRAP_SPI0_CSN	AUD_DAT_MOSI0	JTAG Function	
default=PU	default=PD	AP_JTAG	MD_JTAG
HI	LO	N/A	N/A
HI	HI (by.ext. PU)	SPI0+EINT8	SPI1+SPI3
LO (by.ext. PD)	LO	SPI0+EINT8	N/A
LO (by.ext. PD)	HI (by.ext. PU)	MSDC1	N/A

Note 12-4: PWRAP_SPI0_MI / PWRAP_SPI0_MO is DDR type feature in bootstrap

PWRAP_SPI0_MI	PWRAP_SPI0_MO	Booting interface	
default=PU	default=PD	DDR	MSDC0 pin mux
LO (by.ext. PD)	LO	LPDDR3	follow LPDDR3 Ref SCH.
LO (by.ext. PD)	HI (by.ext. PU)	N/A	N/A
HI	LO	LPDDR4X	follow LP4X/LP4 Ref SCH.
HI	HI (by.ext. PU)	LPDDR4	follow LP4X/LP4 Ref SCH.

Note 12-5: Please set unused IO pins in NC

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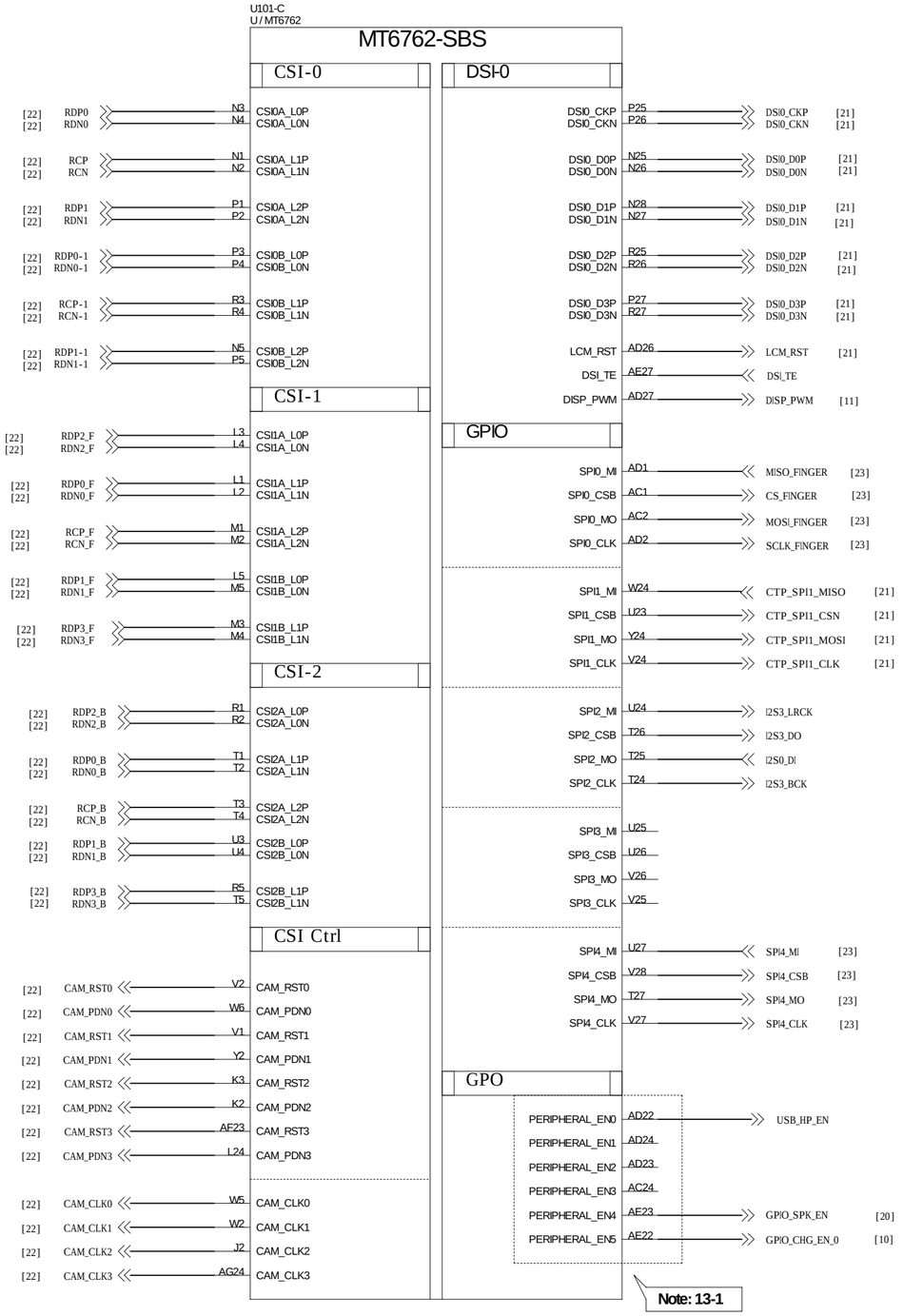

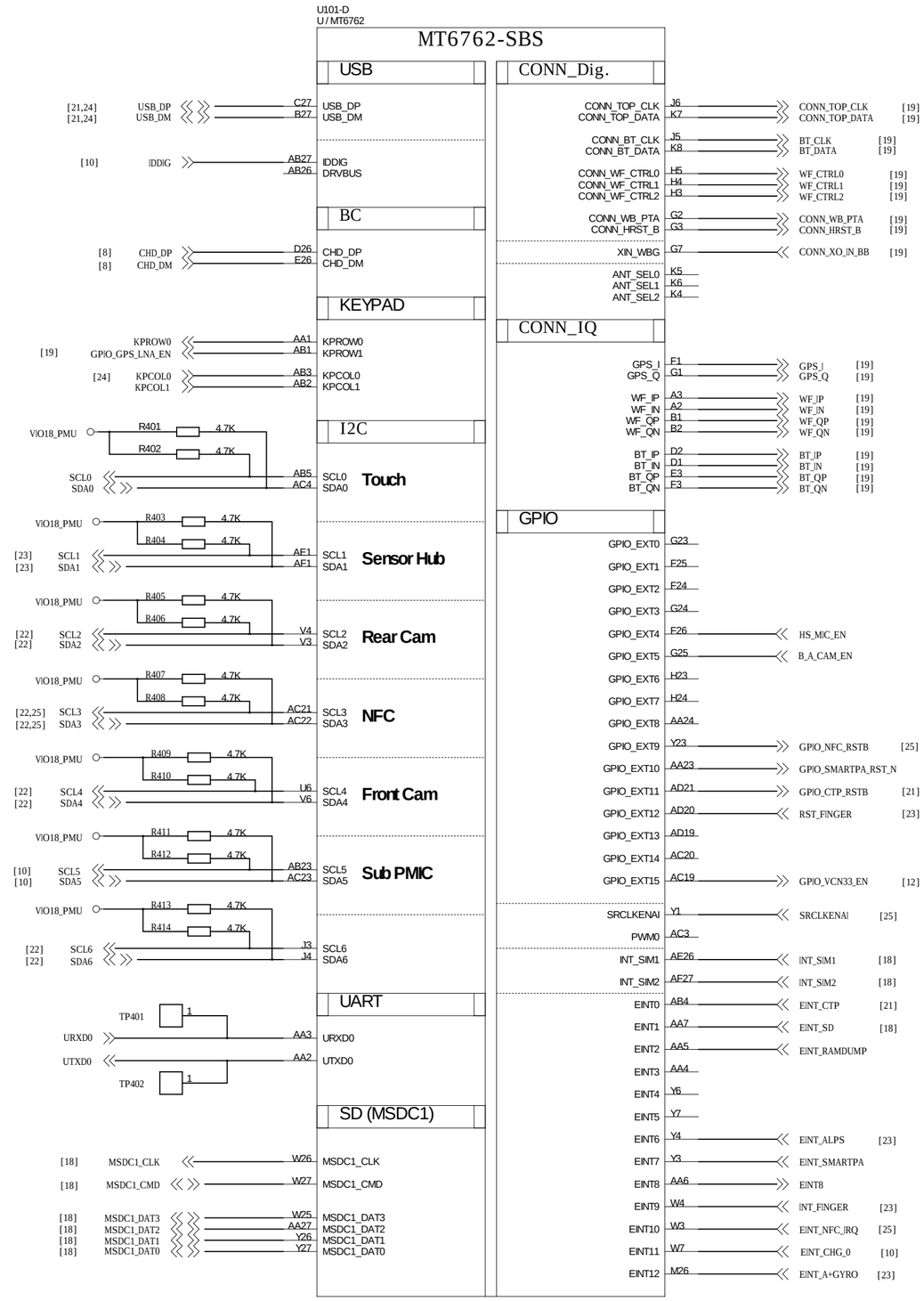

Schematic design notice of "13_BB_2" page.

Note 13-1: The enable pin of acoustic or optoelectronic devices (e.g. SPK AMP/Backlight/Charger OCP/OVP) suggest to use Peripheral_EN[0:5]

Note 13-2: MIPI CSI unused pin can be floating, but need correct SW setting
If use other GPIOs as enable pin, suggest to reserve 0201 NC to GND

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EMI_DDR

[17]	EMI0_DQ0	C13	EMI0_DQ0	EMI0_CS0_N	A9	EMI0_CS0	[17]
[17]	EMI0_DQ1	C15	EMI0_DQ1	EMI0_CS1_N	E8	EMI0_CS1	[17]
[17]	EMI0_DQ2	C14	EMI0_DQ2				
[17]	EMI0_DQ3	E15	EMI0_DQ3	EMI0_CKE0	D8	EMI0_CKE0	[17]
[17]	EMI0_DQ4	B15	EMI0_DQ4	EMI0_CKE1	E7	EMI0_CKE1	[17]
[17]	EMI0_DQ5	D15	EMI0_DQ5				
[17]	EMI0_DQ6	E16	EMI0_DQ6	EMI0_DM0	B16	EMI0_DMI0	[17]
[17]	EMI0_DQ7	B17	EMI0_DQ7	EMI0_DM1	C17	EMI0_DMI1	[17]
[17]	EMI0_DQ8	A17	EMI0_DQ8	EMI0_DM2	E10	EMI0_DMI2	[17]
[17]	EMI0_DQ9	E18	EMI0_DQ9	EMI0_DM3	B19	EMI0_DMI3	[17]
[17]	EMI0_DQ10	F18	EMI0_DQ10				
[17]	EMI0_DQ11	C18	EMI0_DQ11	EMI0_CK_T	F9	EMI0_CK_T	[17]
[17]	EMI0_DQ12	D19	EMI0_DQ12	EMI0_CK_C	F9	EMI0_CK_C	[17]
[17]	EMI0_DQ13	E19	EMI0_DQ13				
[17]	EMI0_DQ14	C19	EMI0_DQ14	EMI0_DQS0_C	E14	EMI0_DQS0_C	[17]
[17]	EMI0_DQ15	A19	EMI0_DQ15	EMI0_DQS0_T	D14	EMI0_DQS0_T	[17]
[17]	EMI0_DQ16	D10	EMI0_DQ16				
[17]	EMI0_DQ17	C11	EMI0_DQ17	EMI0_DQS1_C	D17	EMI0_DQS1_C	[17]
[17]	EMI0_DQ18	C10	EMI0_DQ18	EMI0_DQS1_T	E17	EMI0_DQS1_T	[17]
[17]	EMI0_DQ19	D12	EMI0_DQ19				
[17]	EMI0_DQ20	B13	EMI0_DQ20	EMI0_DQS2_C	E13	EMI0_DQS2_C	[17]
[17]	EMI0_DQ21	B11	EMI0_DQ21	EMI0_DQS2_T	F13	EMI0_DQS2_T	[17]
[17]	EMI0_DQ22	B12	EMI0_DQ22	EMI0_DQS3_C	E22	EMI0_DQS3_C	[17]
[17]	EMI0_DQ23	E11	EMI0_DQ23	EMI0_DQS3_T	D22	EMI0_DQS3_T	[17]
[17]	EMI0_DQ24	D20	EMI0_DQ24				
[17]	EMI0_DQ25	E20	EMI0_DQ25				
[17]	EMI0_DQ26	E21	EMI0_DQ26	EMI0_CA0	B8	EMI0_CA0	[17]
[17]	EMI0_DQ27	D21	EMI0_DQ27	EMI0_CA1	B7	EMI0_CA1	[17]
[17]	EMI0_DQ28	B20	EMI0_DQ28	EMI0_CA2	C7	EMI0_CA2	[17]
[17]	EMI0_DQ29	C22	EMI0_DQ29	EMI0_CA3	D6	EMI0_CA3	[17]
[17]	EMI0_DQ30	C21	EMI0_DQ30	EMI0_CA4	B5	EMI0_CA4	[17]
[17]	EMI0_DQ31	A21	EMI0_DQ31	EMI0_CA5	D5	EMI0_CA5	[17]
				EMI0_CA6	C5	EMI0_CA6	[17]
				EMI0_CA7	E6	EMI0_CA7	[17]
[17]	EVREF	F16	VREF_EMI	EMI0_CA8	E5	EMI0_CA8	[17]
		G16	NC	EMI0_CA9	A5	EMI0_CA9	[17]
		E23	NC	NC	A7		
				NC	B9		
				NC	C4		
				NC	C9		
				NC	D4		
				NC	D7		
				NC	D11		
				NC	D18		
	EMI_EXTR	B4	EMI_EXTR				

R501
34.8
D_GND

eMMC (MSDC0)

[17]	MSDC0_DAT7	A26	MSDC0_DAT7	MSDC0_RSTB	C25	MSDC0_RSTB	[17]
[17]	MSDC0_DAT6	B24	MSDC0_DAT6				
[17]	MSDC0_DAT5	B23	MSDC0_DAT5	MSDC0_CMD	B25	MSDC0_CMD	[17]
[17]	MSDC0_DAT4	A23	MSDC0_DAT4				
[17]	MSDC0_DAT3	C24	MSDC0_DAT3	MSDC0_CLK	D25	MSDC0_CLK	[17]
[17]	MSDC0_DAT2	A25	MSDC0_DAT2				
[17]	MSDC0_DAT1	D24	MSDC0_DAT1	MSDC0_DSL	B26	MSDC0_DSL	[17]
[17]	MSDC0_DAT0	C26	MSDC0_DAT0				

Title	14_BB_3
Size	A0
	MTK Confidential
Date:	Monday, November 18, 2019
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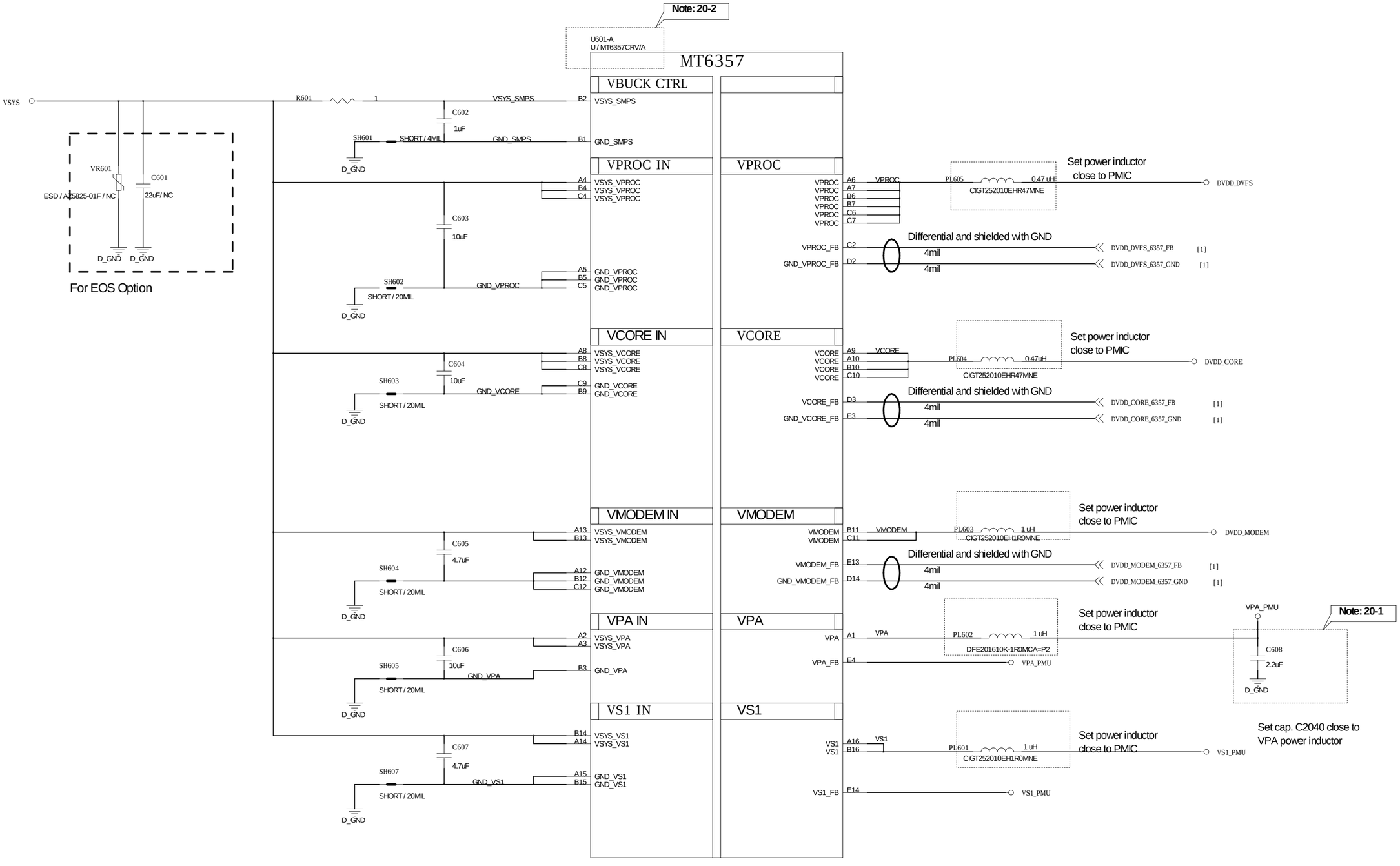


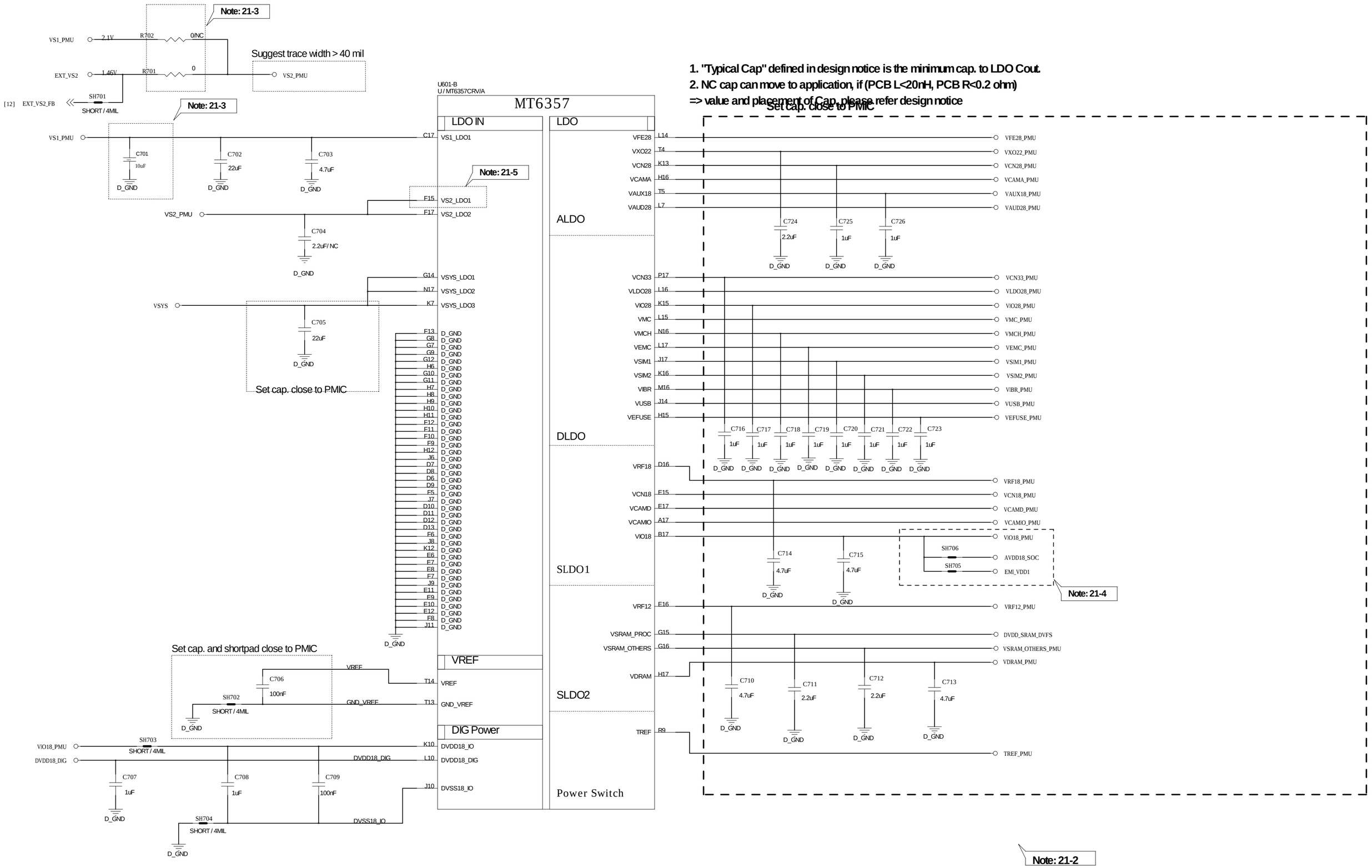
Schematic design notice of "20_POWER_MT6357_Buck"

Note 20-1: C2040, please choose 0402 size

Note 20-2: PMIC Part number notice for MT6765/62/61 platform

MTK Platform	PMIC
MT6765 / 62	MT6357 CRV
MT6761	MT6357 MRV

Title	20_POWER_MT6357-Buck
Size	A0
	MTK Confidential
Date:	Monday, November 18, 2019
Sheet	6 of 27



Schematic design notice of "21_POWER_MT6357_LDO"

Note 21-1:
If these power trace can meet LDO layout constraint, these CAP can be NC or removed.
Please refer to MT6357 design notice.

Note 21-2: Output cap range please follow MT6357CRV LDO design notice

Note 21-3: Ext Buck BOM option

	Ext. buck option	
	w/ EXT VS2 Buck	w/o EXT VS2 Buck
C701	10uF(0402)	22uF(0603)
R701	0-ohm , 0603	NC
R702	NC	0-ohm , 0603

Note 21-4: Please set SH2101 close to C2141, making star connection between VIO18_PMU and AVDD18_SOC near to LDO cap. C2141
Please also refer to MT6357 design notice for further detail design information

Note 21-5: Please connect VS2_LDO1(F15) to VS1_PMU if voltage applied to VCAMD(E17) > 1.3 V

Title: 21_POWER_MT6357-LDO
Size: A0
MTK Confidential
Date: Monday, November 18, 2019
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U601-C
U / MT6357CRV/A

MT6357

Control I/F

[10,24] PWRKEY — D801 D / NSR01L30MXT5G — PWRKEY_PMIC — R4 PWRKEY
[24] HOMEKEY — N4 FCHR_ENB
[3] SYSRSTB — R5 RESETB
[3,10] WATCHDOG — T8 WDTRSTB_IN
D_GND — R801 200K — UVLO_VTH — N3 UVLO_VTH

[3] SRCLKENA0 — N7 SRCLKEN_IN0
[3,13] SRCLKENA1 — N8 SRCLKEN_IN1

EXT_PMIC_EN1 — M5 EXT_PMIC_EN1
[12] EXT_PMIC_EN2 — N5 EXT_PMIC_EN2
M6 EXT_PMIC_PG

[3] PWRAP_SPI0_CSN — R8 SPI_CSN
[3] PWRAP_SPI0_CK — M8 SPI_CLK
[3] PWRAP_SPI0_MO — M7 SPI_MOSI
[3] PWRAP_SPI0_MI — M9 SPI_MISO

P5 PMU_TESTMODE
P9 FSOURCE
D_GND

Charger I/F

Set cap. close to PMIC

VSYS — SH801 SHORT / 4MIL — N9 VSYSSNS
VSYS — SH802 SHORT / 4MIL — M13 BATSNS
VBAT — SH803 SHORT / 4MIL — N13 ISENSE
Differential
Note: 22-5
C801 1uF D_GND
C802 100nF D_GND
C803 100nF D_GND
BATON — R13 BATON
VCDT — T11 VCDT
CHRLDO — R11 CHRLDO
P13 VDRV

VBUS
R802 330K 1%
[10] BATON
R803 39K 1% D_GND
VCDT rating: 1.268V

VBUS — R804 7.5 K — C804 1uF D_GND
Set resistor and cap. close to PMIC

[4] CHD_DM — M10 CHG_DM
[4] CHD_DP — M11 CHG_DP
Differential
N12 PCHR_LED

Gauge

[10] CS_P — T10 CS_P
[10] CS_N — R10 CS_N
Differential

ISINK

L12 ISINK1

RTC

Set cap. close to chip

VRTC28 — R12 — C811 100nF D_GND
VRTC28 — R811 1.5K — C812 22uF D_GND

RTC32K_1V8_0 — P14 — RTC32K_CK [3]
RTC32K_1V8_1 — R15
RTC32K_2V8 — P11

DCXO

Note: 22-2

AVSS22_XO — M2 AVSS22_XO — D_GND
AVSS22_XOBUF — P1 AVSS22_XOBUF — D_GND
AVSS22_XOBUF — R1
AVSS22_XO_ISO — N2 AVSS22_XO_ISO — D_GND
AVSS22_XO_ISO — P2

XO_SOC — R3 XO_SOC — R810 0 — PMIC_CLK_BB [3]
XO_CEL — T1 XO_CEL — R809 0 — PMIC_CLK_RF [13]
XO_WCN — P3 XO_WCN — R808 0 — PMIC_CLK_WCN [19]
XO_NFC — R2 XO_NFC — R807 0 — PMIC_CLK_NFC [25]
XO_EXT — T2

C807 NC D_GND
C808 NC D_GND
C809 NC D_GND
C810 NC D_GND

XTAL1 — M1 — XTAL1 [8]
XTAL2 — N1 — XTAL2 [8]

Note: 22-4

AUXADC

R806 0 — VAUX18_PMU

AVDD18_AUXADC — R7 — C806 1uF
AVSS18_AUXADC — P7 — SH804 SHORT / 4MIL — D_GND
AUXADC_VIN — T7 — C805 100nF
Set cap. close to PMIC

AVSS18_AUXADC
AUXADC_VIN — 3mil trace width
AVDD18_AUXADC — 3mil trace width
3mil trace width

R805 100 K 1%

X801
TMS / OZ26030001
RT1 (4) — XT2 (3) — XTAL2 [8]
[8] XTAL1 — XT1 (1) — RT2 (2)
3mil trace width
AVSS18_AUXADC
3mil trace width

Note: 22-1

Route AVDD18_AUXADC, AUXADC_VIN, and AVSS18_AUXADC with 3mils width traces and well GND shielding

Schematic design notice of "22_POWER_MT6357-IF"

Note 22-1: Please implement 2520 & 2016 Size TMS PCB co-layout.

Note 22-2: Please refer to MT6762_MT6357 Co-Clock Design Notice for co-layout guide

Note 22-3:
1. Please Connect P1 and R1 ball first and then to GND
2. Please Connect P2 and N2 ball first and then to GND
3. Please connect DCXO GND to main GND by independent L1-2 GND via.;
DO NOT connect it through L1 GND

Note 22-4: Please follow MT6762_MT6357 Co-Clock Design Notice for Layout guide of VAUX18, then R8101 can use 0 ohm to replace BEAD.

Note 22-5: Please connect to battery connector

Title: 22_POWER_MT6357-IF
Size: A0
MTK Confidential
Date: Monday, November 18, 2019 Sheet 8 of 27

U601-D
U / MT6357CRV/A

MT6357

AUDIO IF

[3]	AUD_CLK_MISO	R16	AUD_CLK_MISO
[3]	AUD_DAT_MISO0	T17	AUD_DAT_MISO0
[3]	AUD_DAT_MISO1	R17	AUD_DAT_MISO1
[3]	AUD_SYNC_MISO	T16	AUD_SYNC_MISO
[3]	AUD_CLK_MOSI	P16	AUD_CLK_MOSI
[3]	AUD_DAT_MOSI0	P15	AUD_DAT_MOSI0
[3]	AUD_DAT_MOSI1	N14	AUD_DAT_MOSI1
[3]	AUD_SYNC_MOSI	M14	AUD_SYNC_MOSI

AUDIO INPUT

[20]	AU_VIN0_P	K3	AU_VIN0_P
[20]	AU_VIN0_N	K4	AU_VIN0_N
[20]	AU_VIN1_P	K5	AU_VIN1_P
[20]	AU_VIN1_N	L5	AU_VIN1_N
	AU_VIN2_P	J4	AU_VIN2_P
	AU_VIN2_N	J5	AU_VIN2_N

ACCDET

[20]	ACCDET	M4	ACCDET
[20]	HP_EINT	J1	HP_EINT

AUDIO OUTPUT

[20]	AU_HPL	J2	AU_HPL
[20]	AU_REFN	H3	AU_REFN
[20]	AU_HPR	G3	AU_HPR
[20]	AU_LOLP	F4	AU_LOLP
[20]	AU_LOLN	F3	AU_LOLN
[20]	AU_HSP	G6	AU_HSP
[20]	AU_HSN	G5	AU_HSN

C901
1nF
D_GND

Set cap. close to PMIC

- AU_HPL and AU_HPR should be routed as single end signal,
  and be guarded by GND, up and down, left and right respectively
- The suggested layout pattern of AU_HPL/ AU_HPR/ AU_REFN
  is " GND AU_HPL AU_REFN AU_HPR GND"

UL POWER

AVDD28_AUD	K1		VAUD28_PMU
AVSS28_AUD	H5	[20]	AVSS28_AUD
AU_MICBIAS0	L3		AU_MICBIAS0 [20,21]
AU_MICBIAS1	M3		AU_MICBIAS1 [20]

C907 1uF
C905 1uF
C906 1uF
SH902 SHORT / 4MIL
D_GND

Set cap. and shortpad close to PMIC

CHARGE PUMP

AVDD18_AUD	G2	VIO18_PMU
AVSS18_AUD	F2	AVSS_AUD
AU_V18N	D1	AU_V18N
FLYP	F1	FLYP
FLYN	E2	FLYN

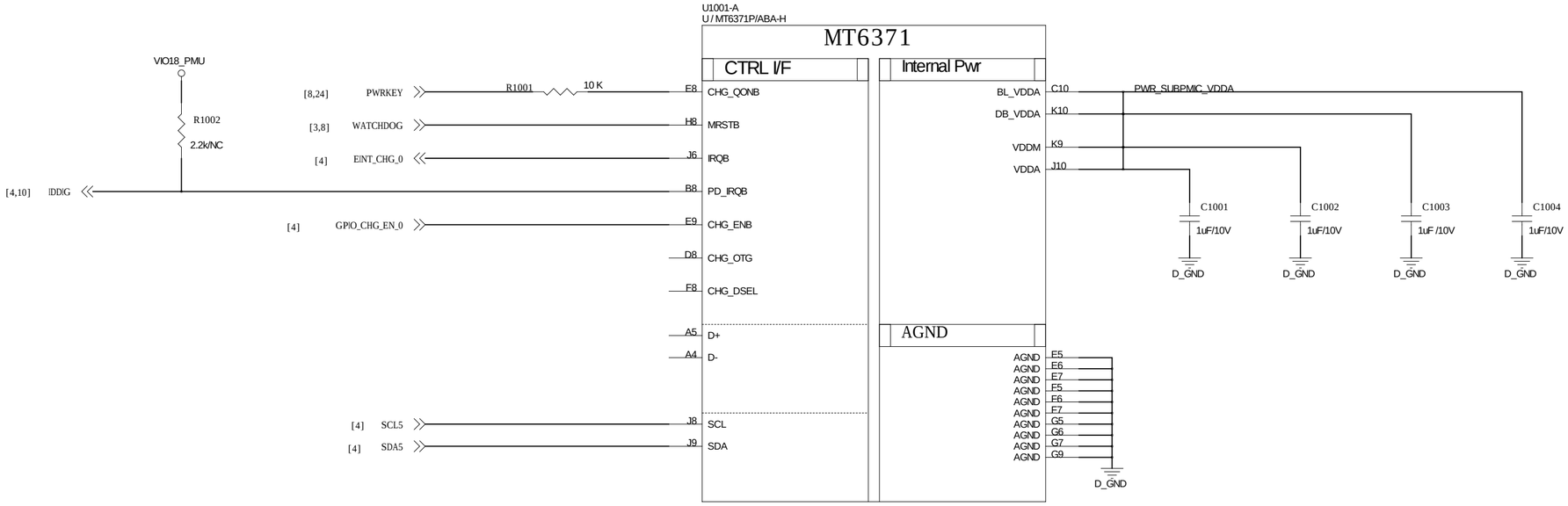
C904 2.2uF
C903 4.7uF
C902 4.7uF
SH901 SHORT / 4MIL
D_GND

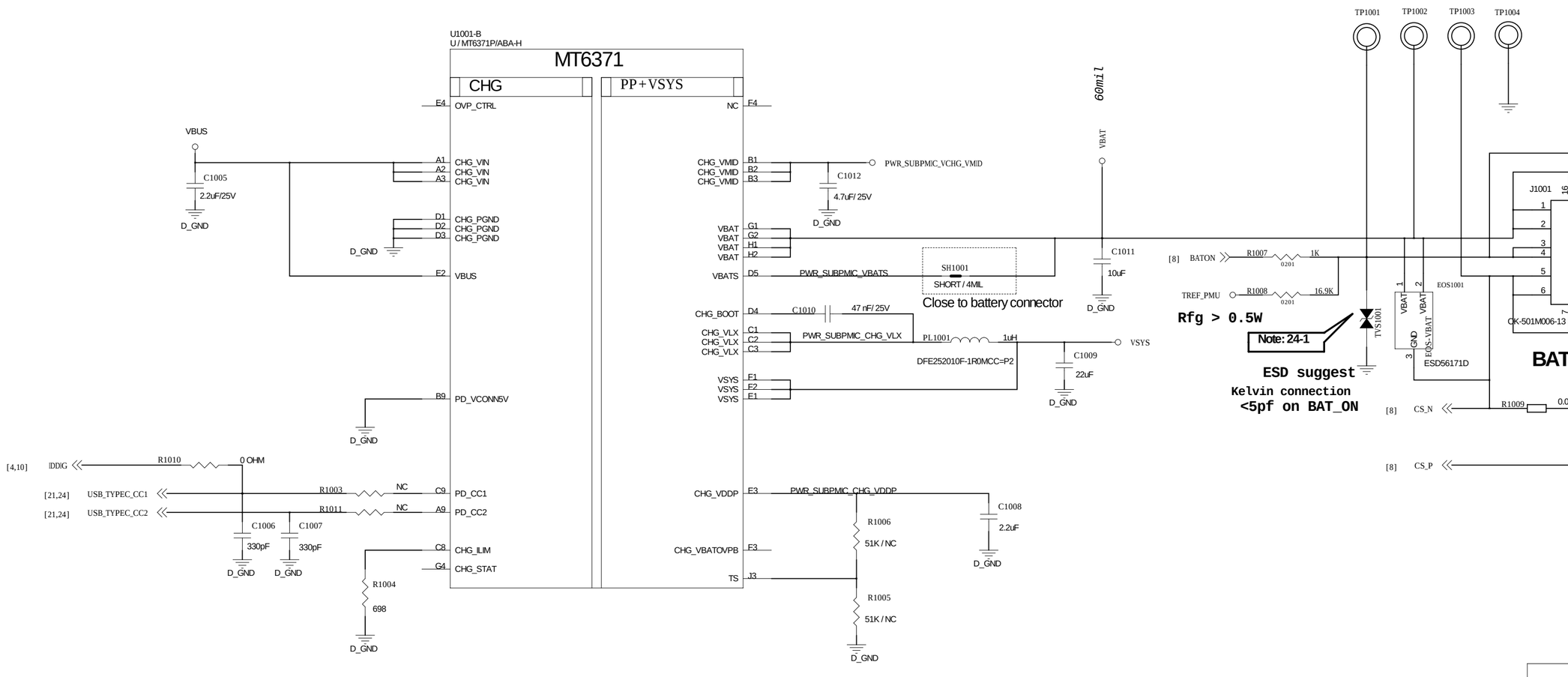
Set cap. close to PMIC

1. AVSS18_AUD is connected to GND in very short trace

2. AVSS18_AUD is connected to de-couple cap of
AVDD18_AUD and AU_V18N with 6mil trace respectively

Title	23_POWER_MT6357-Audio
Size A0	MTK Confidential
Date: Monday, November 18, 2019	Sheet 9 of 27





Title	25_POWER_SubPMIC-General
Size	A0
	MTK Confidential
Date:	Monday, November 18, 2019
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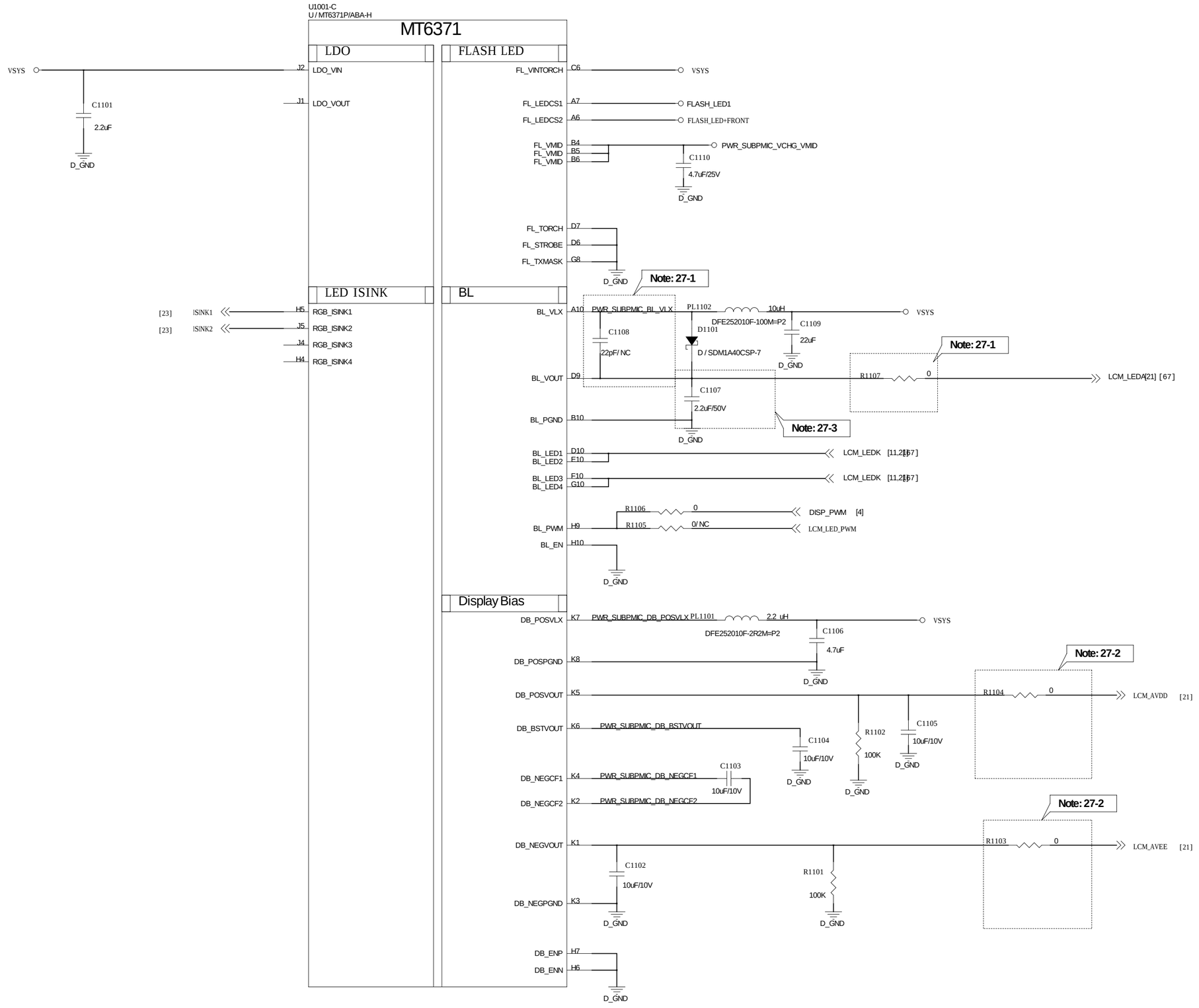

Schematic design notice of "27_POWER_SubPMIC-HV powers" page:

Note 27-1: To minimize RF de-sense, it is recommended to reserve 0-ohm and 0402 cap for BOM fine tuning.

Note 27-2: To minimize RF de-sense, it is recommended to reserve 0-ohm and 0201 cap. for BOM fine tuning.

Note 27-3: C2705 could be replaced with C / 1 / uF / 50V + C / 1 / uF / 50V

Title: 27_POWER_SubPMIC-HV powers
Size: A0
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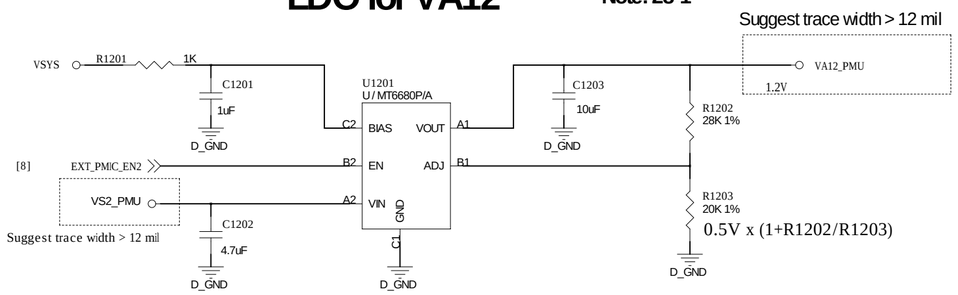
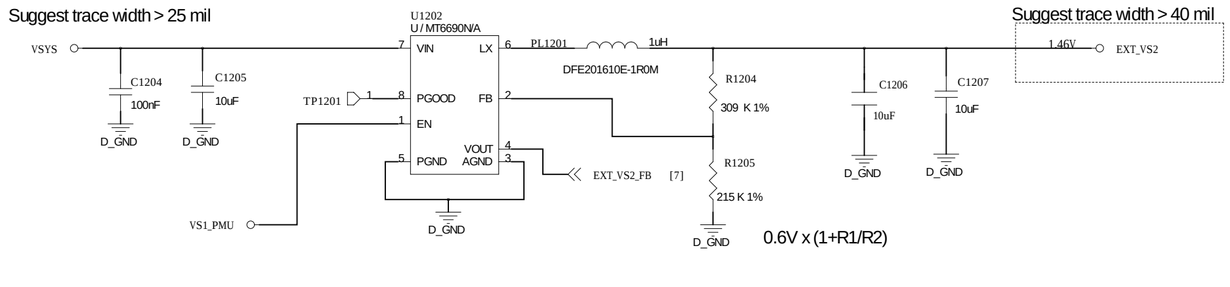
LDO for VA12

Note: 28-1



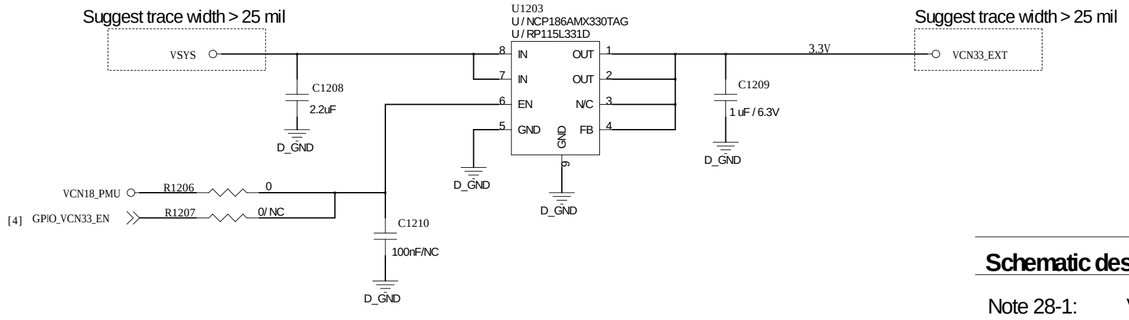
Ext. Bulk for VS2

Note: 28-2



LDO for VCN33

Note: 28-3



Schematic design notice of "28_POWER_ThirdParty-Power"

Note 28-1:	VA12 Layout placement please close to AP
Note 28-2:	VS2 Buck Layout placement please close to PMIC MT6357
Note 28-3:	VCN33 LDO Layout placement please close to MT6631
Note 28-4:	1.MT6691OOP/A Buck Layout Placement please close to LP4X/LP4 2.MT6691ZXP/A Buck Layout Placement please close to LP4X 3.If DRAM Application is LPDDR4 , MT6691ZXP/A NC
Note 28-5:	U2810 LDO Layout Placement Please close to LPDDR4X/LPDDR4 VDD1 power ball
Note 28-6:	For EMI_VDD2_FB and EMI_VDDQ_FB, please follow MMD rule

Title: 28_POWER_ThirdParty_Powers

Size: A0

MTK Confidential

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[16] RF_B12B17_DRX_RFIC
[16] RF_B8_DRX_RFIC
[16] RF_B20_DRX_RFIC
[16] RF_B5_DRX_RFIC
[16] RF_B34B39_DRX_RFIC
[16] RF_B3_DRX_RFIC
[16] RF_B39_B39B41_CA_DRX_RFIC
[16] RF_B38B41_DRX_RFIC
[16] RF_B40_DRX_RFIC
[16] RF_B1B4_DRX_RFIC
[16] RF_B7_DRX_RFIC
[16] RF_B2_DRX_RFIC

RF_B2_PRX_RFIC [15]
RF_B7_PRX_RFIC [15]
RF_B1B4_PRX_RFIC [15]
RF_B40_PRX_RFIC [14]
RF_B38B41_PRX_RFIC [14]
RF_B39_B39B41_CA_PRX_RFIC [14]
RF_B3_PRX_RFIC [15]
RF_B34B39_PRX_RFIC [15]
RF_B5_PRX_RFIC [15]
RF_B20_PRX_RFIC [15]
RF_B8_PRX_RFIC [15]
RF_B12B17_PRX_RFIC [15]

Attenuator for Detector

6dB Attenuator

[13] RF_TXDET1_RFIC — R1303 37.4 — RF_TXDET1 [15]
R1302 150 D_GND
R1304 150 D_GND

U1301

DRX: NC, DRX14, DRX13, DRX12, DRX11, DRX10, DRX9, DRX8, DRX7, DRX6, DRX5, DRX4, DRX3, DRX2, DRX1
PRX: NC, PRX14, PRX13, PRX12, PRX11, PRX10, PRX9, PRX8, PRX7, PRX6, PRX5, PRX4, PRX3, PRX2, PRX1

Only PRX1-8 can be assigned to GSM HB

MT6177

TXO: TX_UHB, TX_HB1, TX_HB2 → RF_HB2_TX_RFIC [14], TX_MB1, TX_MB2 → RF_MB2_TX_RFIC [14], TX_MB3 → RF_MB3_TX_RFIC [15], TX_LB1 → RF_LB1_TX_RFIC [14], TX_LB2, TX_LB3 → RF_LB3_TX_RFIC [15], TX_LB4, TXDET1 → RF_TXDET1_RFIC [13]

Power: VDD_TXHV, VDD_SXLF, VDD_SXLV, VDD_RXLV, VDD_RXHV, VIO

VIO18_RFIC, VRF18_RXHV, VRF12_RXLV, VRF12_SXLV, VRF18_SXLF, VRF18_TXHV

C1301–C1306 100nF D_GND

XOI → PMIC_CLK_RF [8]
EN_BB → SRCLKENA1 [3,8]
TMEAS
RCAL → R1301 2K 1% D_GND

GND: B7, C3–C7, C8–C10, D3–D10, F3–F5, E8–E10, F2–F8, F9–F10, E11–E12, G2–G3, G5–G10, H2–H3, H6–H9, H10, J3, J6–J9

DETIF: DET_IP0, DET_IN0, DET_QP0, DET_QN0
DRX(I/Q): DRX_BB_Q1, DRX_BB_I1, DRX_BB_Q0, DRX_BB_I0
PRX(I/Q): PRX_BB_Q1, PRX_BB_I1, PRX_BB_Q0, PRX_BB_I0
TX(I/Q): TX_BB_QN0, TX_BB_QP0, TX_BB_IN0, TX_BB_IP0
BSI: BSI_0_EN, BSI_0_CK, BSI_0_D0, BSI_0_D1, GND

MT6177W/ACA

[3] LTE_DET_BB_IP0
[3] LTE_DET_BB_IN0
[3] LTE_DET_BB_QP0
[3] LTE_DET_BB_QN0
[3] LTE_DRX_BB_Q1
[3] LTE_DRX_BB_I1
[3] LTE_DRX_BB_Q0
[3] LTE_DRX_BB_I0
[3] LTE_PRX_BB_Q1
[3] LTE_PRX_BB_I1
[3] LTE_PRX_BB_Q0
[3] LTE_PRX_BB_I0

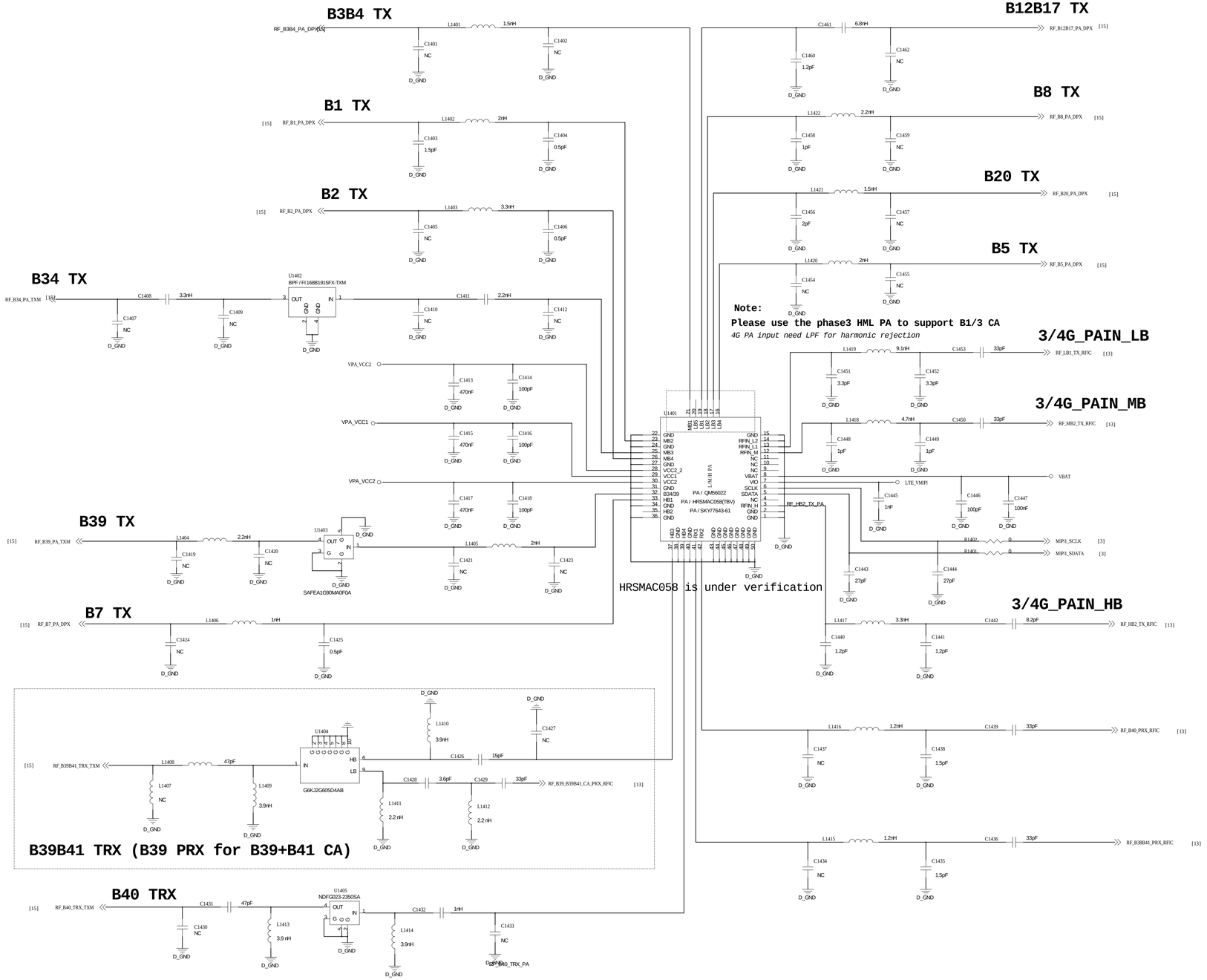
RFIC0_BSI_D1 [3]
RFIC0_BSI_D0 [3]
RFIC0_BSI_CK [3]
RFIC0_BSI_EN [3]
LTE_TX_BB_IP0 [3]
LTE_TX_BB_IN0 [3]
LTE_TX_BB_QP0 [3]
LTE_TX_BB_QN0 [3]

4.7uF close to RFIC

Power For MT6177

VRF18_TXHV — R1305 0 — VRF18_PMU
VRF18_RXHV — R1306 0
VRF18_SXLF — R1307 0
C1307 4.7uF D_GND
VRF12_RXLV — R1308 0 — VRF12_PMU
VRF12_SXLV — R1309 0
C1308 4.7uF D_GND
VIO18_RFIC — R1310 0 — VIO18_PMU

Title	31_RF_MT6177_Pin_Out
Size A0	MTK Confidential
Date: Friday, November 09, 2018	Sheet 13 of 27



Title	32_RF_MT6177M_RF_TX
Size	A0
	MTK Confidential
Date:	Monday, November 18, 2019
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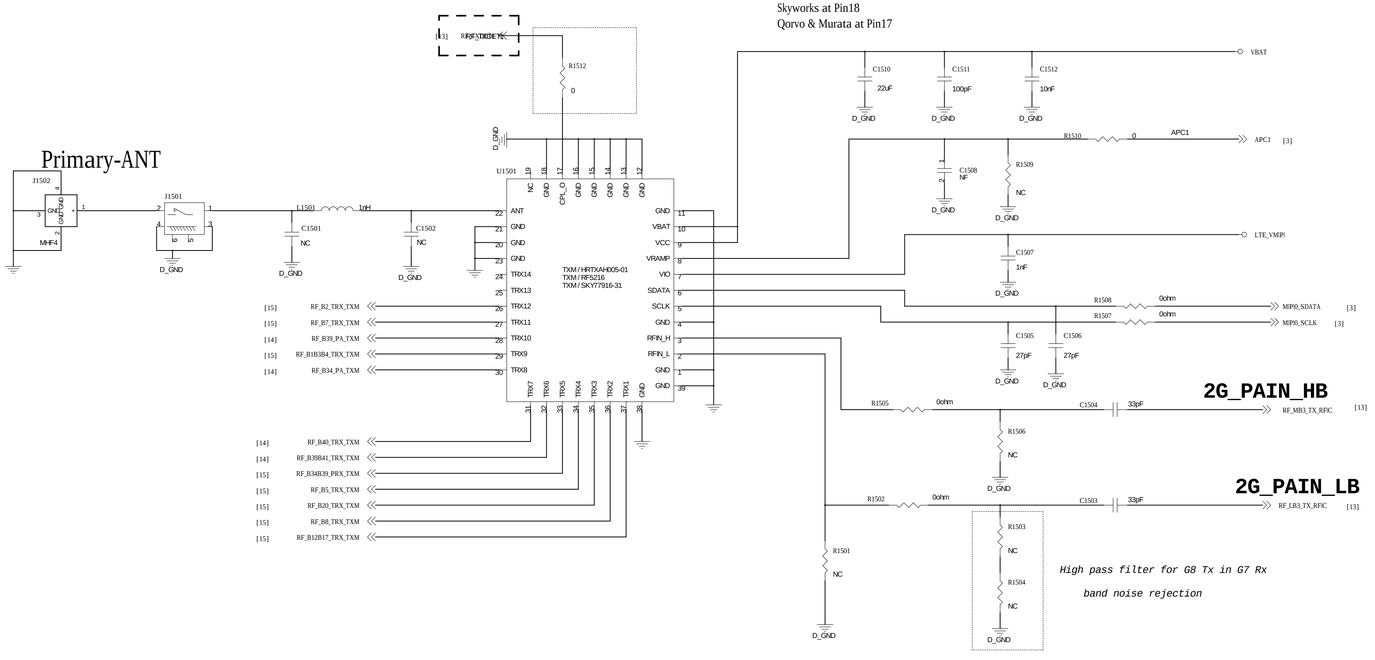
HMLB_Primary-ANT

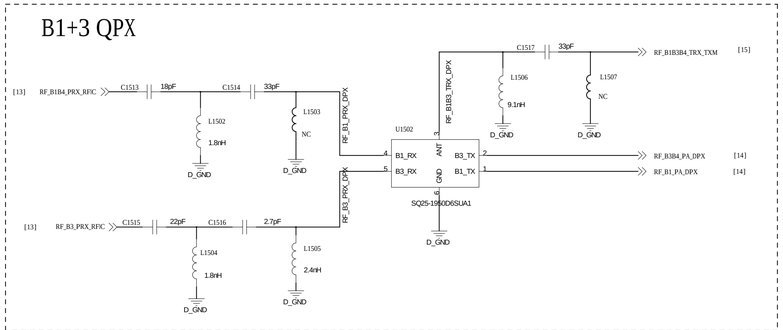
Note for CPL pin:(Reserved 0ohm for Co-layout)
Skyworks at Pin18
Qorvo & Murata at Pin17

Primary-ANT

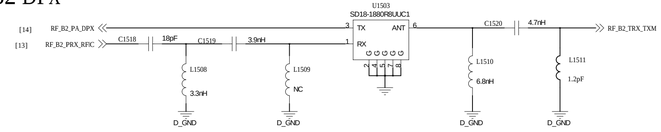


High pass filter for G8 Tx in G7 Rx band noise rejection

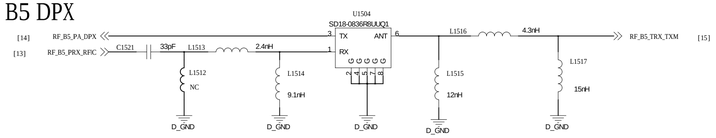
B1+3 QPX



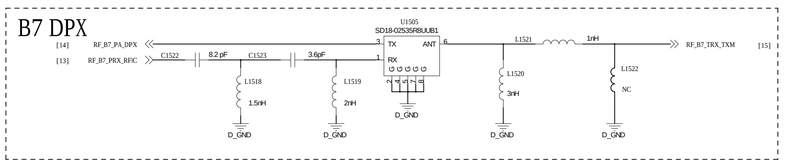
B2 DPX



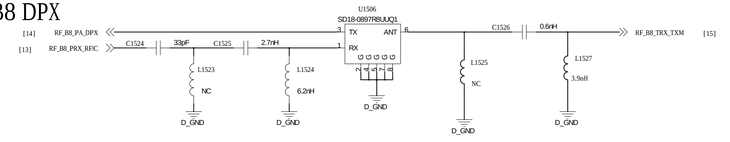
B5 DPX



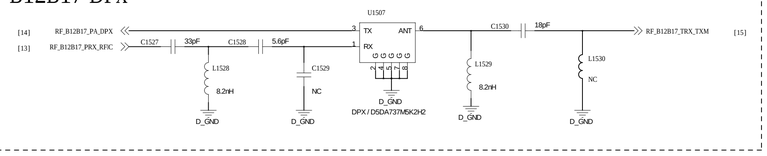
B7 DPX



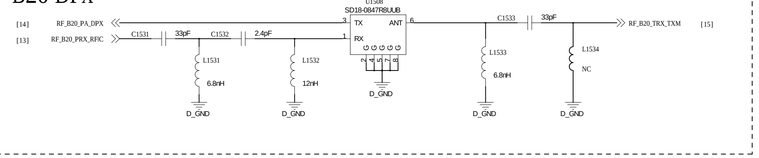
B8 DPX



B12B17 DPX

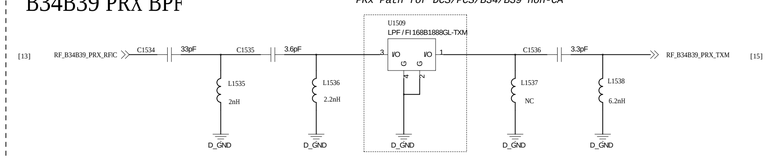


B20 DPX



B34B39 PRX BPF

Band Pass Filter for SAWless Application.
PRx Path for DCS/PCS/B34/B39 non-CA



Title	33_RF_MT6177M_RF_PRX
Size	A0
	MTK Confidential
Date:	Monday, November 18, 2019
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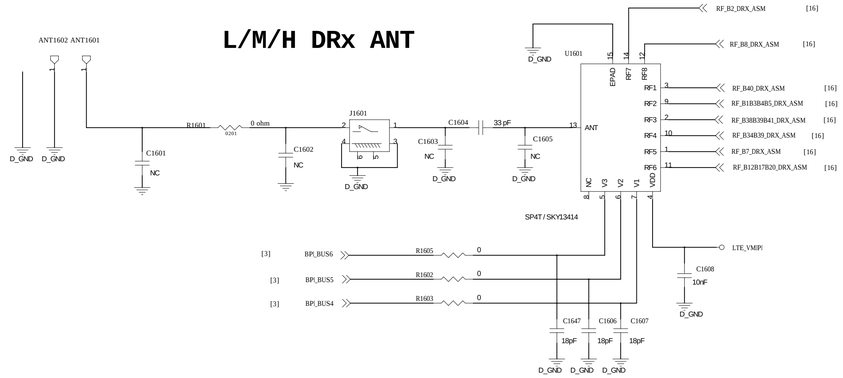
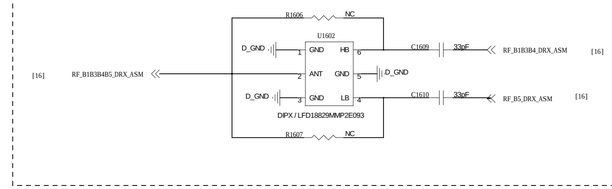
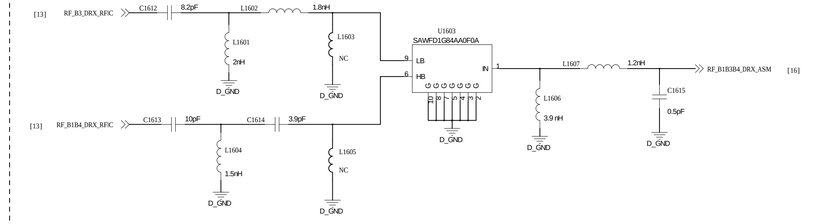
L/M/H DRx ANT



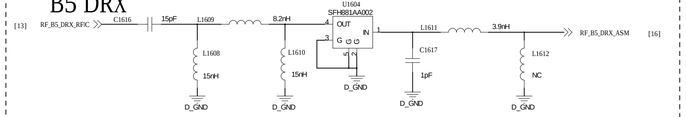
B1/B3/B5 Diplexer



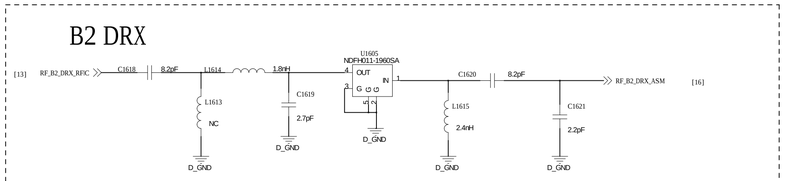
B1/3 DRX+SAW



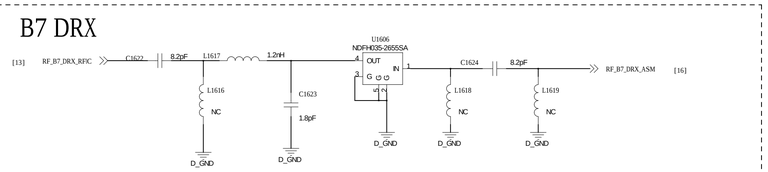
B5 DRX



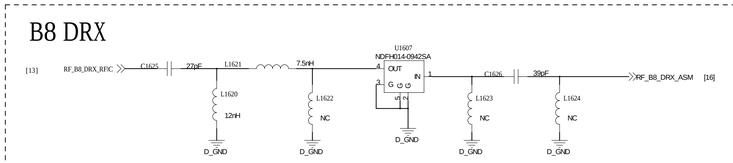
B2 DRX



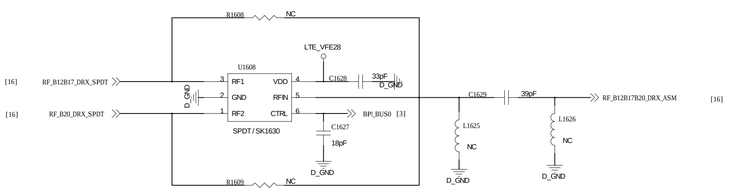
B7 DRX



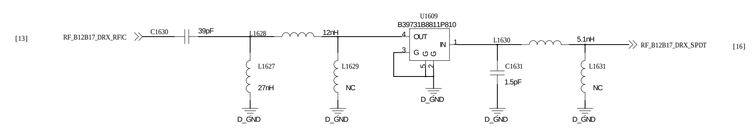
B8 DRX



B12B17-B20 SPDT

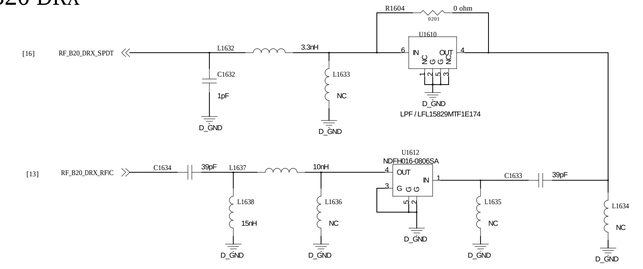


B12B17 DRX

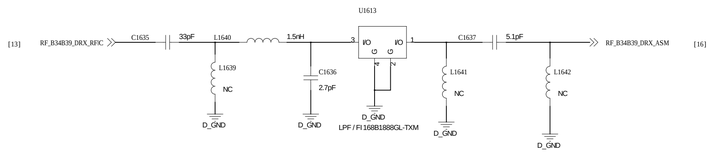


B20 DRX

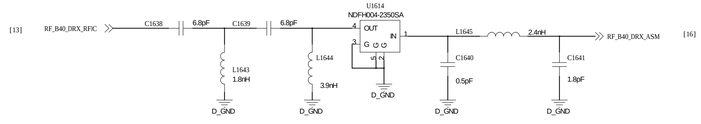
Note: LPF for Coexistence with WIFI



B34B39 DRX

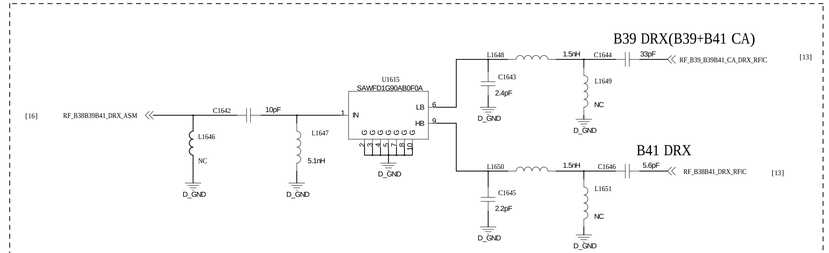


B40 DRX



B39 DRX(B39+B41 CA)

B41 DRX



Title	34_RF_MT6177M_RF_DRX
Size A0	MTK Confidential
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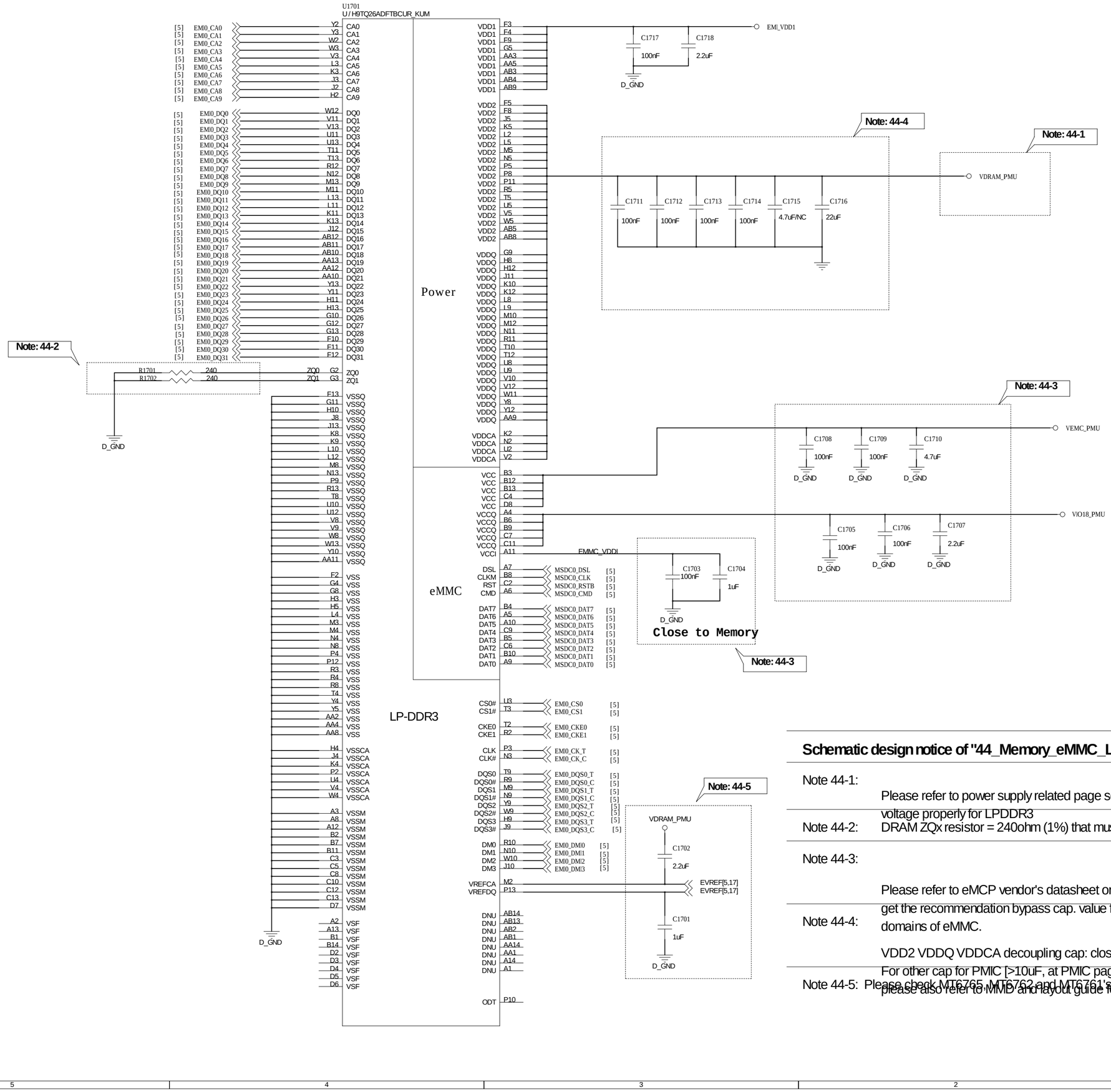

Schematic design notice of "44_Memory_eMMC_LPDDR3"

Note 44-1:
Please refer to power supply related page select VDRAM1 output voltage properly for LPDDR3

Note 44-2: DRAM ZQx resistor = 240ohm (1%) that must be connected to GND

Note 44-3:
Please refer to eMCP vendor's datasheet or MTK common design notice to get the recommendation bypass cap. value for VCC/VCCQ/VDDI power domains of eMMC.

Note 44-4:
VDD2 VDDQ VDDCA decoupling cap: closed to DRAM ball.
For other cap for PMIC [>10uF, at PMIC page]:
please also refer to MMD and layout guide for placement.

Note 44-5: Please check MT6765, MT6762 and MT6761's capacitor value.

Title	44_Memory_eMMC_LP4X_LP4
Size	A0
	MTK Confidential
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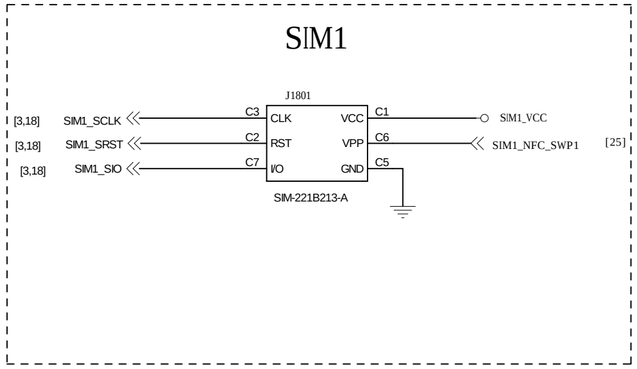

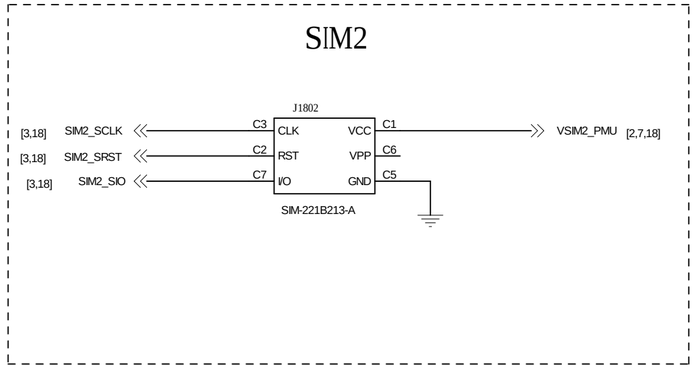

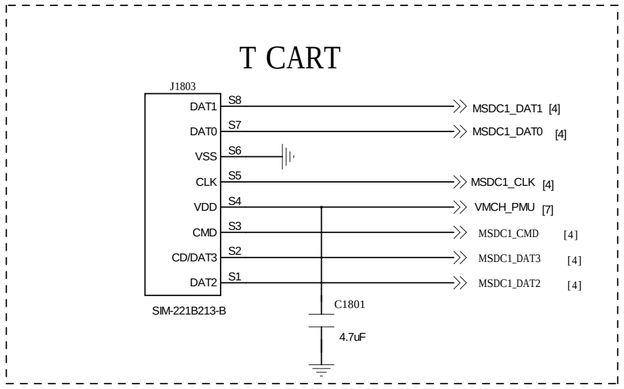

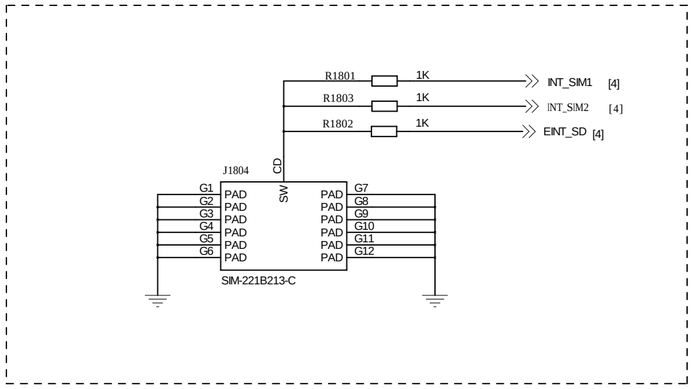

Schematic design notice of "46_MEMORY_SD Card" page.

Note 46-1: For better ESD performance, please select suitable components for system protection.

Title	46_Memory_SD Card
Size	A0
	MTK Confidential
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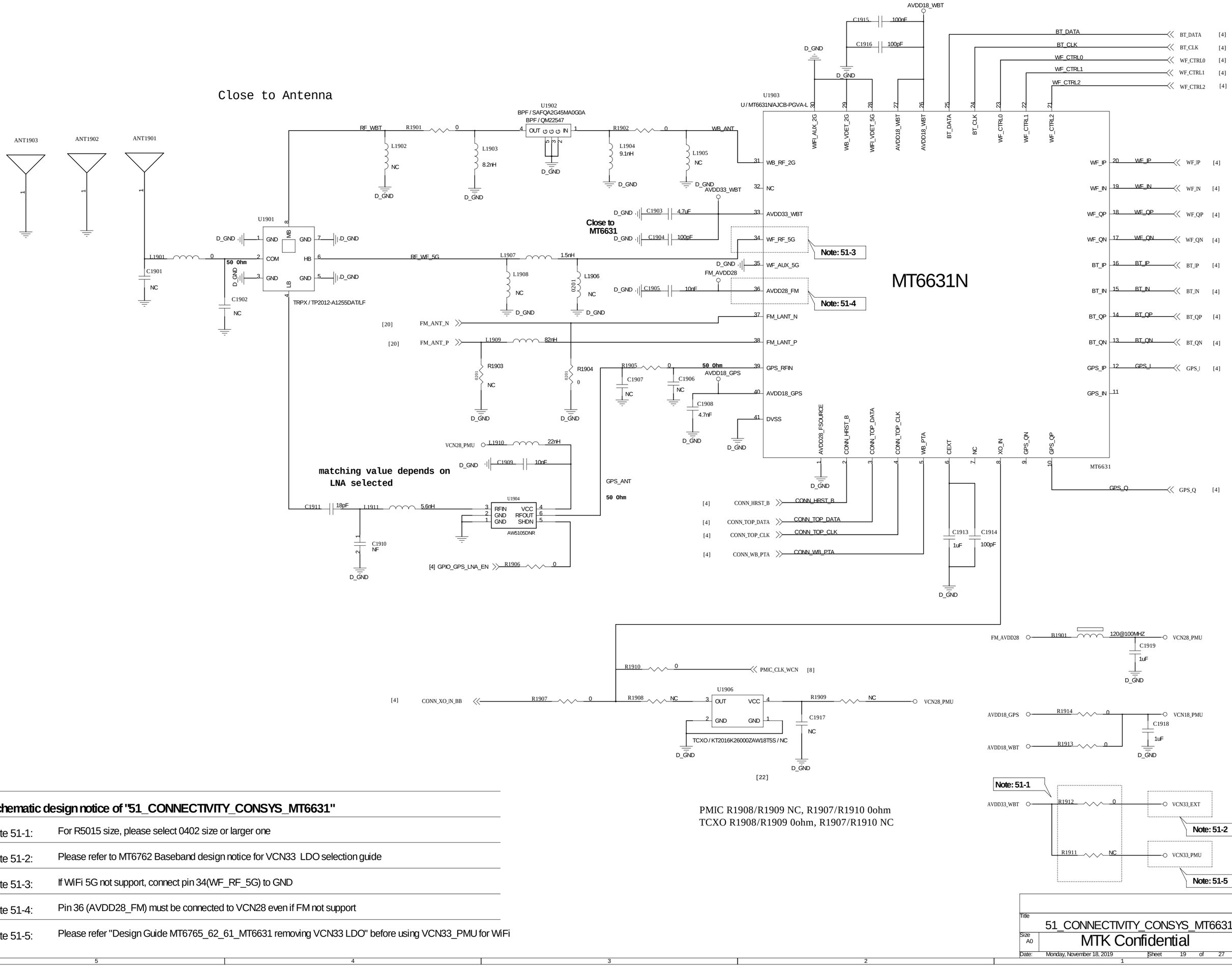

PMIC R1908/R1909 NC, R1907/R1910 0ohm
TCXO R1908/R1909 0ohm, R1907/R1910 NC

Schematic design notice of "51_CONNECTIVITY_CONSYS_MT6631"

Note 51-1:	For R5015 size, please select 0402 size or larger one
Note 51-2:	Please refer to MT6762 Baseband design notice for VCN33 LDO selection guide
Note 51-3:	If WiFi 5G not support, connect pin 34(WF_RF_5G) to GND
Note 51-4:	Pin 36 (AVDD28_FM) must be connected to VCN28 even if FM not support
Note 51-5:	Please refer "Design Guide MT6765_62_61_MT6631 removing VCN33 LDO" before using VCN33_PMU for WiFi

Title: 51_CONNECTIVITY_CONSYS_MT6631
Size: A0
MTK Confidential
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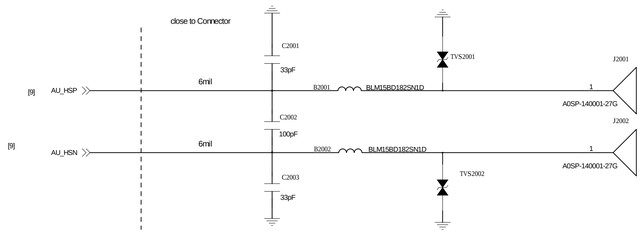
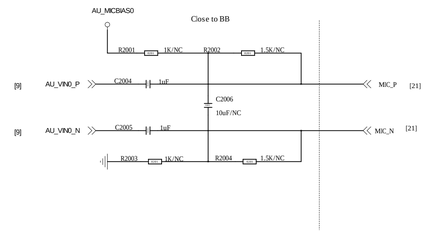
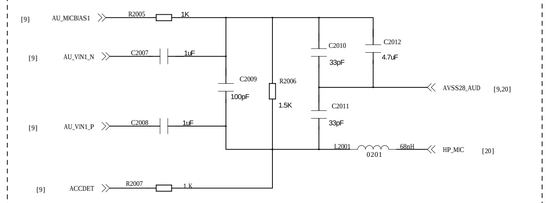
RECEIVER

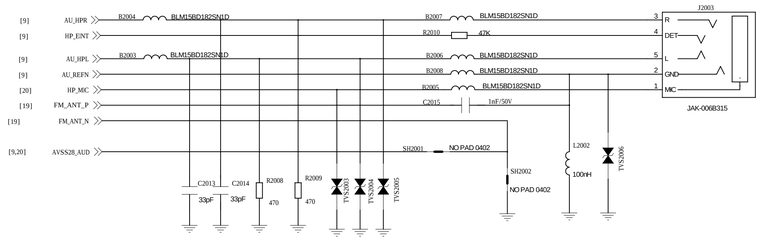


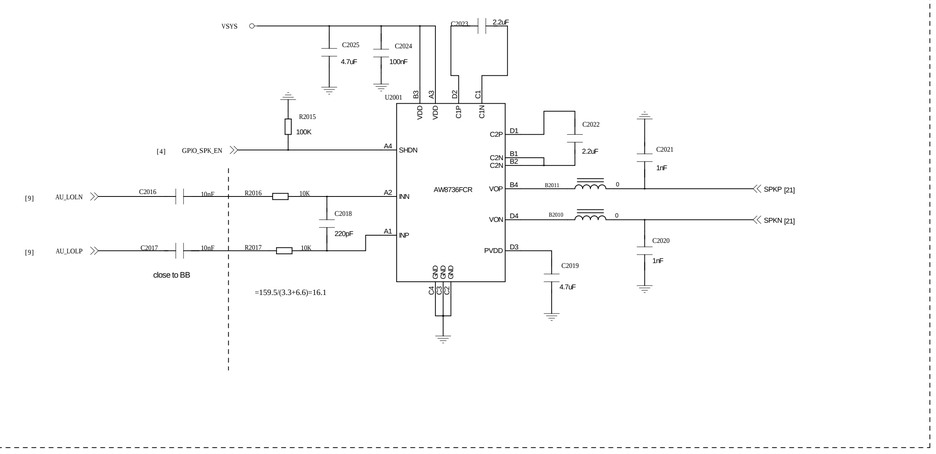
HANDSET MIC



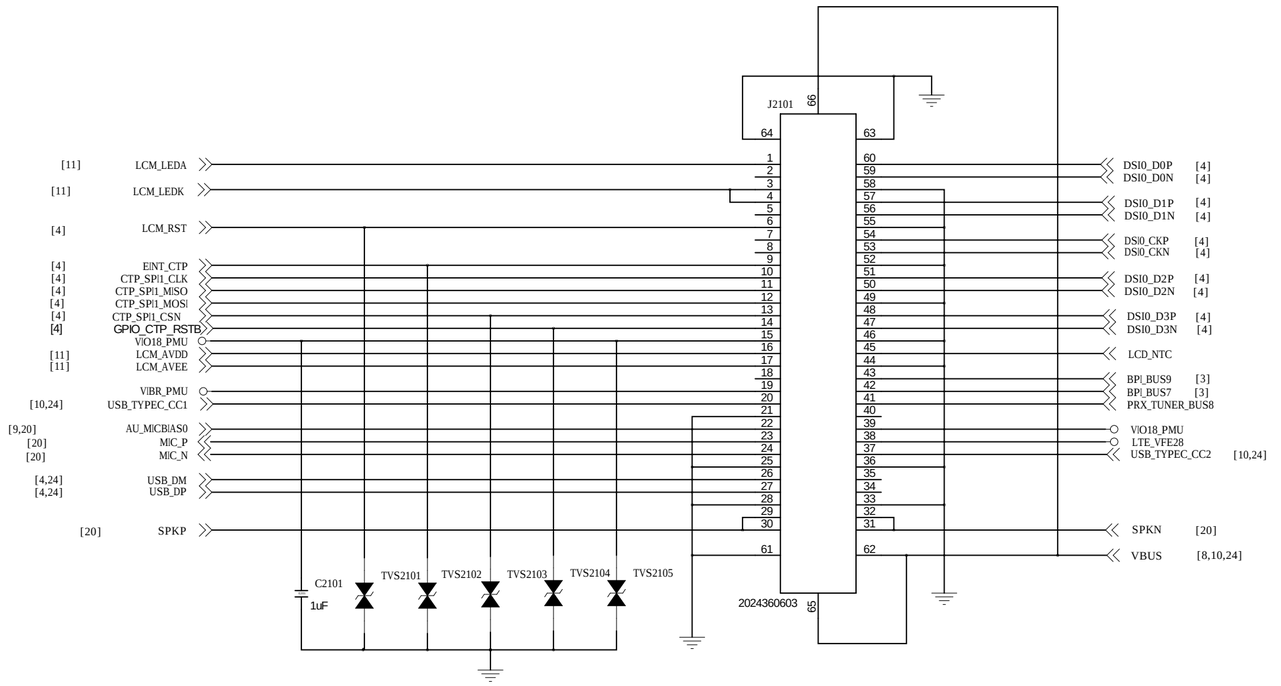


HEADSET





DRAWN BY <Drawn By>	PROJECT <TITLE>	TITLE 20_PERI_AUDIO
CHECKED BY	SIZE A0	VER <REV>
	SHEET 20 of 27	2021/10/25



Schematic design notice of "67_PERI_LCD_CTP" page.

Note 67-1: It is recommended to reserve common-mode choke to prevent RF de-sense, the max. cap loading of common-mode choke must be less than 3pF.

Title	67_PERI_LCD_CTP
Size A0	MTK Confidential
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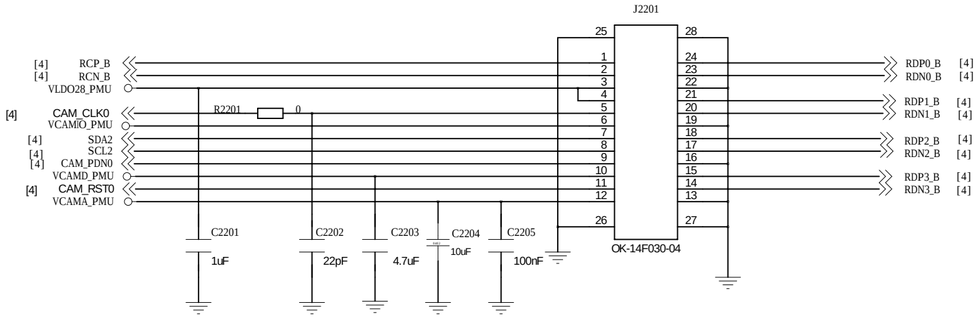
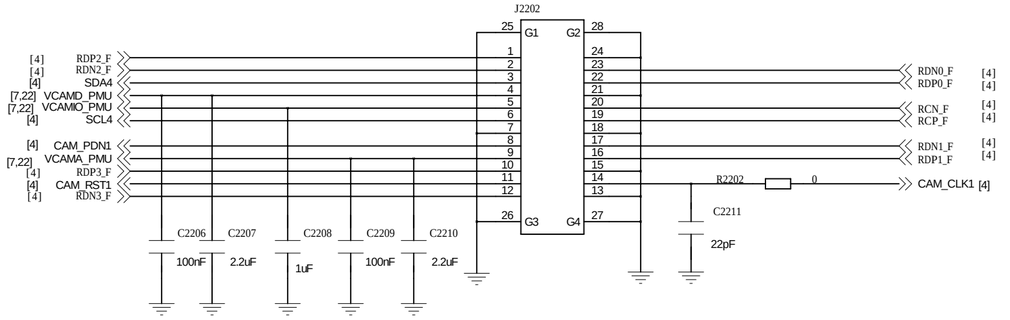
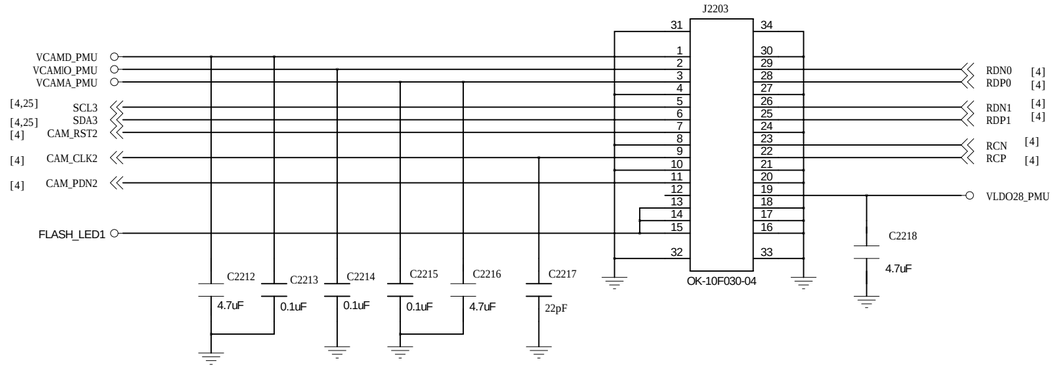
MAIN CAMERA



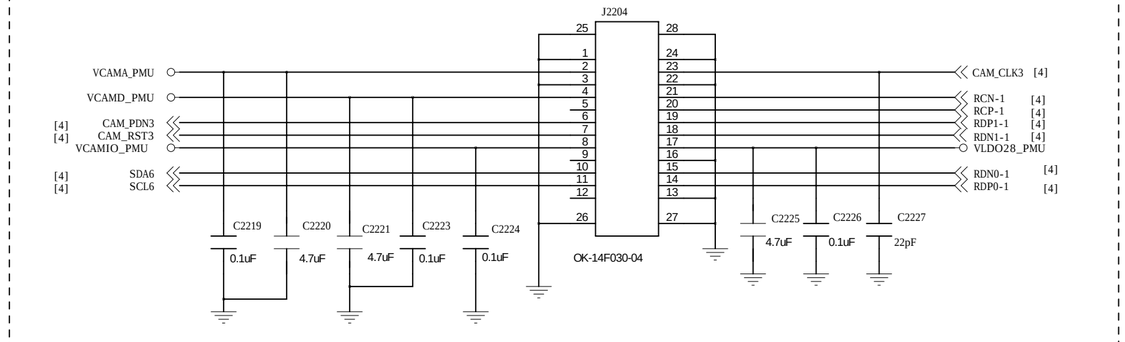
FRONT CAMERA

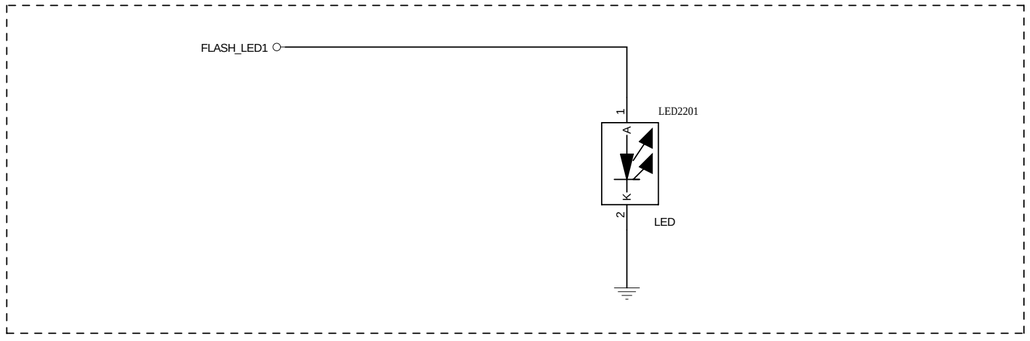


SUB_CAMERA(500M)



SUB_CAMERA(200M)





Schematic design notice of "69_PERI_CAMERA" page.

Note 69-1:

It is recommended to reserve common-mode choke to prevent RF de-sense,
the max. cap loading of common-mode choke must be less than 3pF.

Note 69-2: It is recommended to reserve 0-ohm and cap. for BOM fine tune to minimize RF de-sense.

Title	69_PERI_CAMERA
Size A0	MTK Confidential
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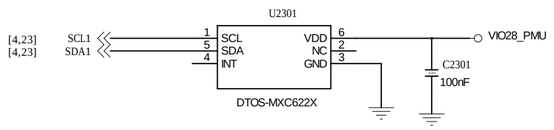
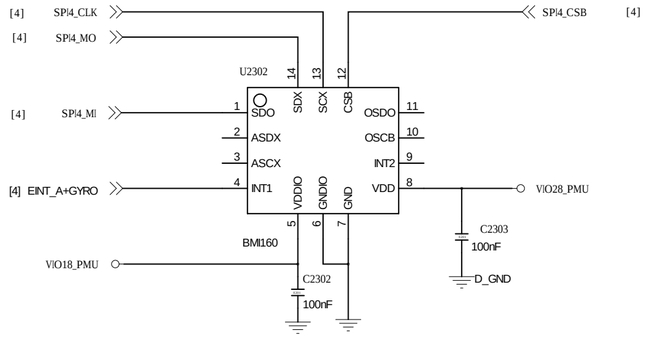
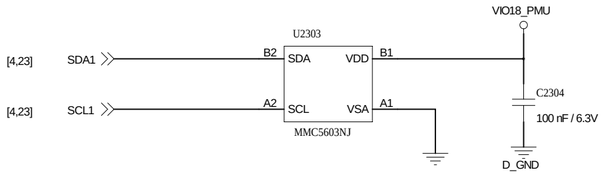
G-ESNSOR



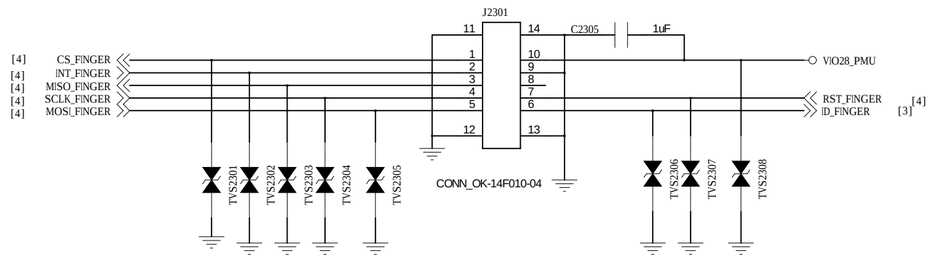
ACC+Gyro Sensor



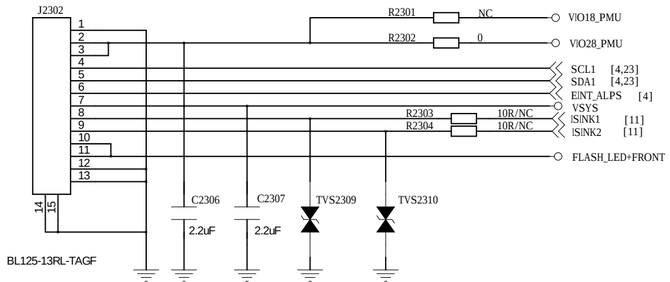
M-Sensor



FINGER SENSOR



ALPS_SENSOR



Title	77_PERI_SENSORS_MEMs_ALS/PS
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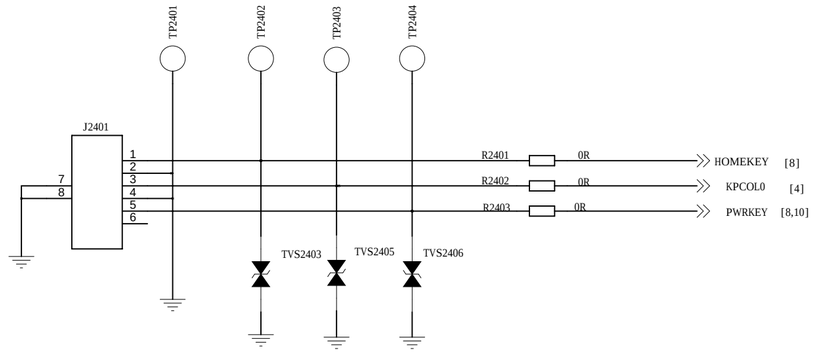
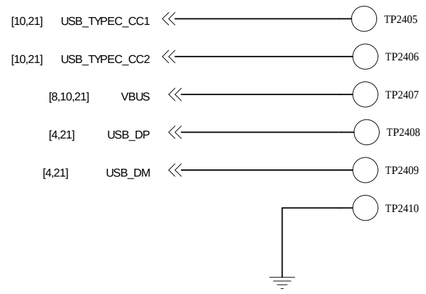
SIDE KEY





Schematic design notice of "71_PERI_USB 2.0" page.

Note 71-1:

For better ESD or surge performance we need choose suitable device for system protection. Please refer to [Surge device selection guide V2.0] provide by MTK.

Title	71_PERI_USB 2.0
Size A0	MTK Confidential
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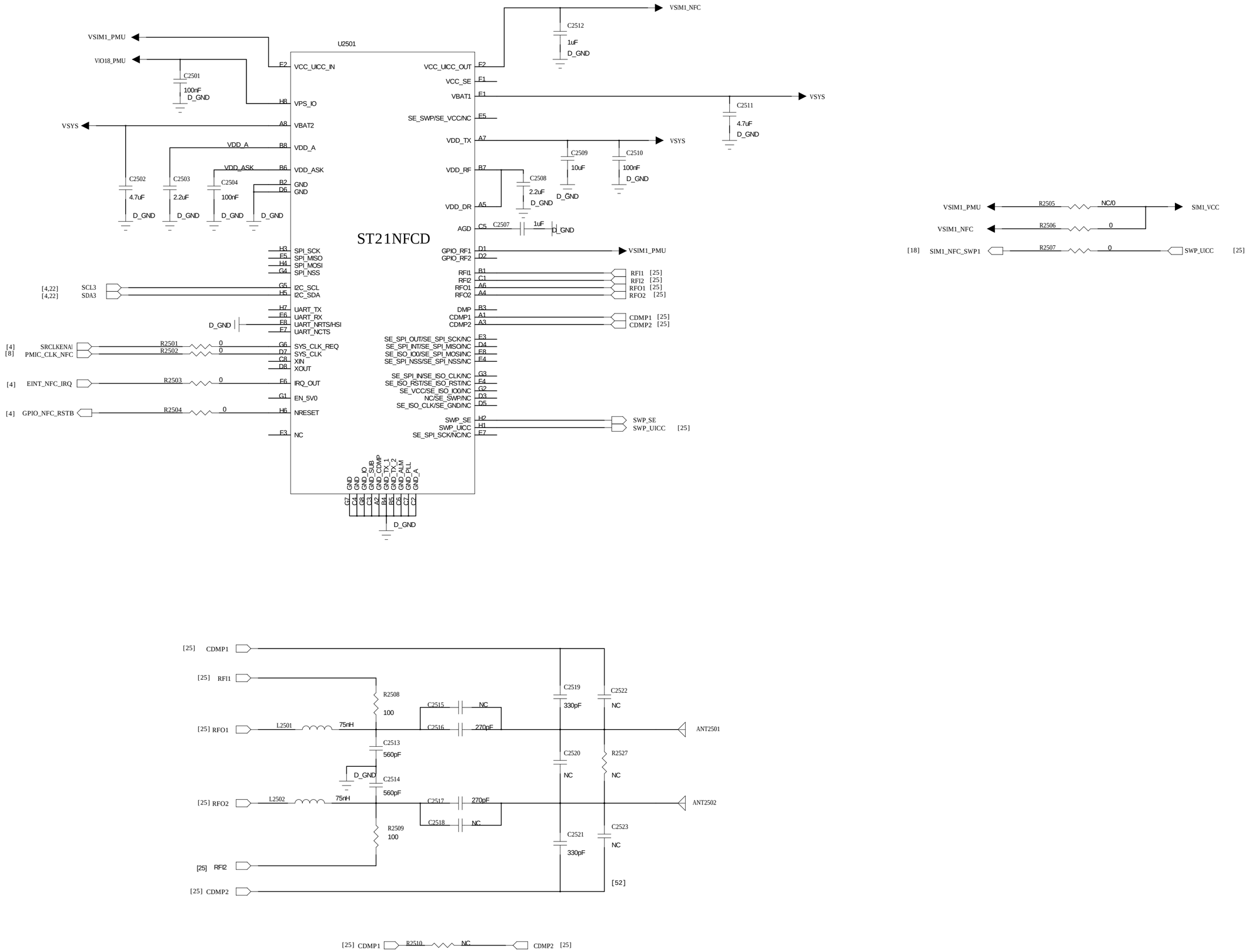

[25] CDMP1 R2510 NC CDMP2 [25]

R2510 is reserved for RF network matching tuning

Title	52_CONNECTIVITY_NFC
Size	A0
	MTK Confidential
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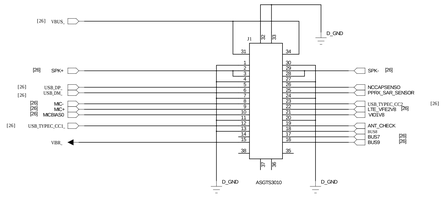
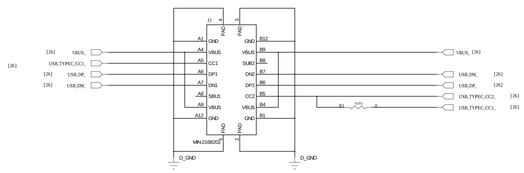
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



USB connector



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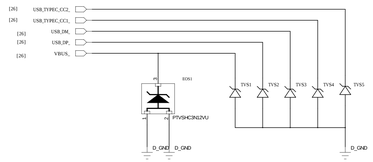
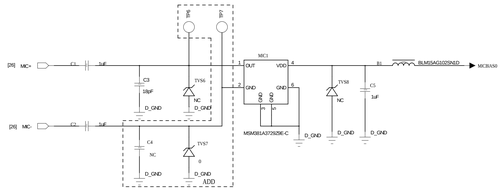
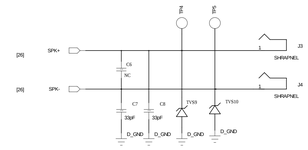
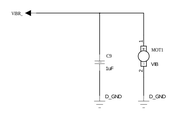


Analog MIC

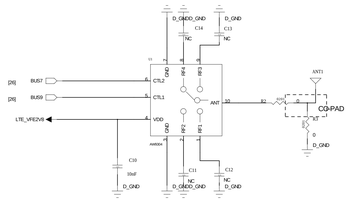


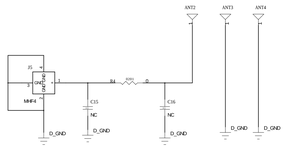
Speaker

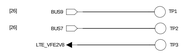




ANT SWITCH







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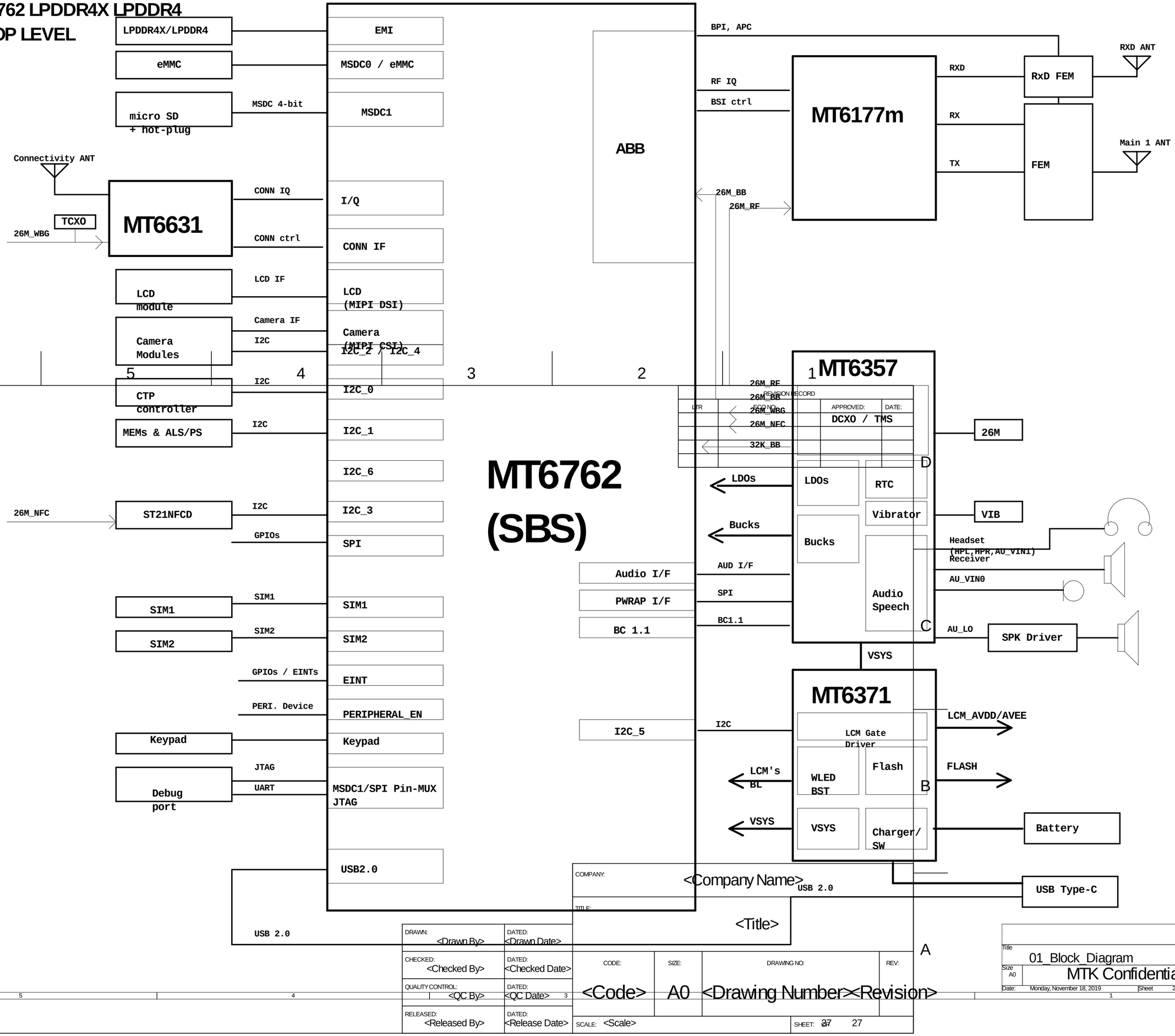
RELEASED: <Released By>	DATED: <Release Date>		
CODE: <Code>	SIZE: A0	DRAWING NO: <Drawing Number><Revision>	REV:
SCALE: <Scale>		SHEET: 26 27	

Project : MT6762 LPDDR4X LPDDR4
REF_SCH TOP LEVEL



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RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>		SHEET: 27 of 27	

Title: 01_Block_Diagram
Size: A0
MTK Confidential
Date: Monday, November 18, 2019 Sheet 27 of 27